

BME – 231

DIGITAL LOGIC DESIGN – EXPERIMENT 7

Design of a Basic MUX/DEMUX Transmission System

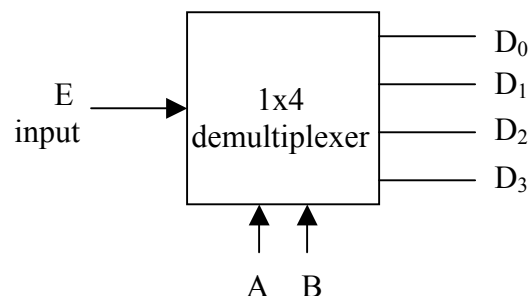
Purpose :

1. Design a 2-bit binary full adder with 3 x 8 decoders.
2. Design 4x16 decoder with 2x4 decoders.
3. Design and implementation of the MUX/DEMUX system for data transmission

Preliminary Work :

1. Read chapter 5 of textbook for decoder, multiplexer and demultiplexer.

“A **demultiplexer** is a circuit that receives information on a single line and transmits this information on one of 2^n possible output lines. The selection of a specific output line is controlled by the bit values of n selection lines. Similar like in the figure 1 below. For example if the selection lines $A=1$ and $B=0$, output D_2 will be the same as the input value E . If you provide data serial at the input, the output data will be serial.”



2. Design a 2-bit full adder with 3 x 8 decoders in Electronics Workbench. It must work similar like in Figure 2. Test your design with $01+01=10$. (Hint: you will use 74138, 4012. Please read “help” about these ICs.)

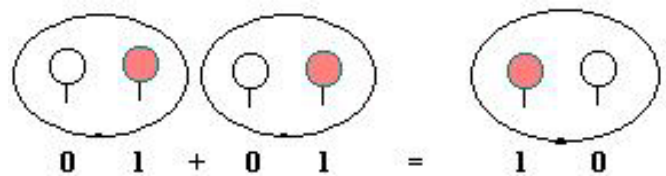


Figure 2

3. Design 4x16 decoder with 2x4 decoders (Hint: you will use 74139 : 2 2x4 decoder) and test your design with 0,1,...,9,A,B,...,F (0000, 0001, ..., 1111) as inputs and observe all outputs 0,1,...,15.
4. Design a data transmission system using Multiplexer and Demultiplexer your design must work similarly blocked design in Figure 3 (Hint: you will use 74156 : 2x4 line decoder with data input, 74153 : 4x1 line data selector/multiplexer with data output, and inverters.)

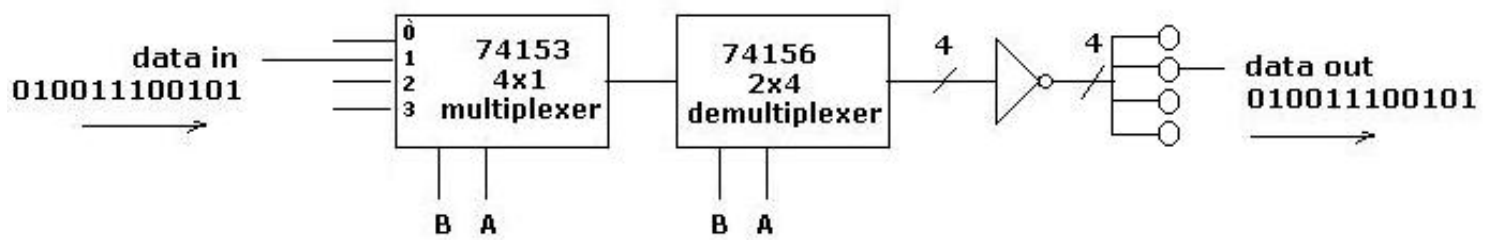


Figure 3

If channel selective bits BAs are constructed, data transmission system will transmit datas from data-in (may be BA=11 and data in channel is I_3 for MUX) to data-out(may be BA=10 and data in channel is D_2 for DEMUX). Do Not Forget that the selective bits are related with input and output channels!

5. Consider the design for 4 bit magnitude comparator and design the 8 bit magnitude comparator.

Experimental Part :

1. Implement your circuit in Preliminary Part 2 design in computer and test it.
2. Implement your design for Preliminary Part 3 in computer, place RED probes at outputs 0-15 and compare it with 74154 : 4x16 decoder outputs for 0-15.
3. Construct the data transmission system as mentioned in Preliminary Part 4 in computer and test your design with data: 001001110101001101 (Hint: you will use word generator for 0s and 1s as 0000 : 0, 0001 : 1). A RED probe will indicate data input of the system and another one indicate output of the system. We expect that the Probes will be red or white at the same time with respect to data.

OR

Construct the circuit that you designed for 8 bit –a byte- magnitude comparator and test your design with word generator 8 bit values. Don't forget the word generator generates words –2 bytes/ 16 bit/ 2x 8 bit-.