

# BME – 231

## DIGITAL LOGIC DESIGN – EXPERIMENT 8

### Synchronous Sequential Logic

#### Purpose :

1. Design sequential logic circuits from state diagrams.
2. Obtain state diagrams from logic circuits

#### Preliminary Work :

1. Read chapter 6 of textbook.
2. A sequential logic circuit has three flip-flops, A,B,C; one input, x; and one output, y. The state diagram for this circuit is shown in Figure 1 below. The circuit is to be designed by treating the unused states as don't care conditions. The final circuit must be analyzed to ensure that it is self correcting.
  - a) Use D flip-flops and appropriate combinational logic construction in your design
  - b) Use JK flip-flops and appropriate combinational logic construction in your design

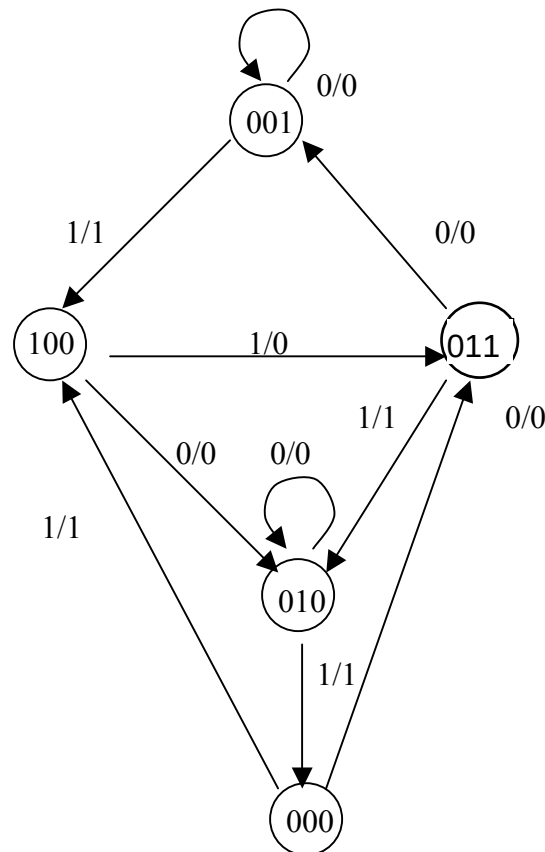


**Figure 1**

3. A sequential circuit has two JK flip-flops, one input x, and one output y. The logic diagram of the circuit is shown in Figure 2. Derive the state table and state diagram of the circuit.

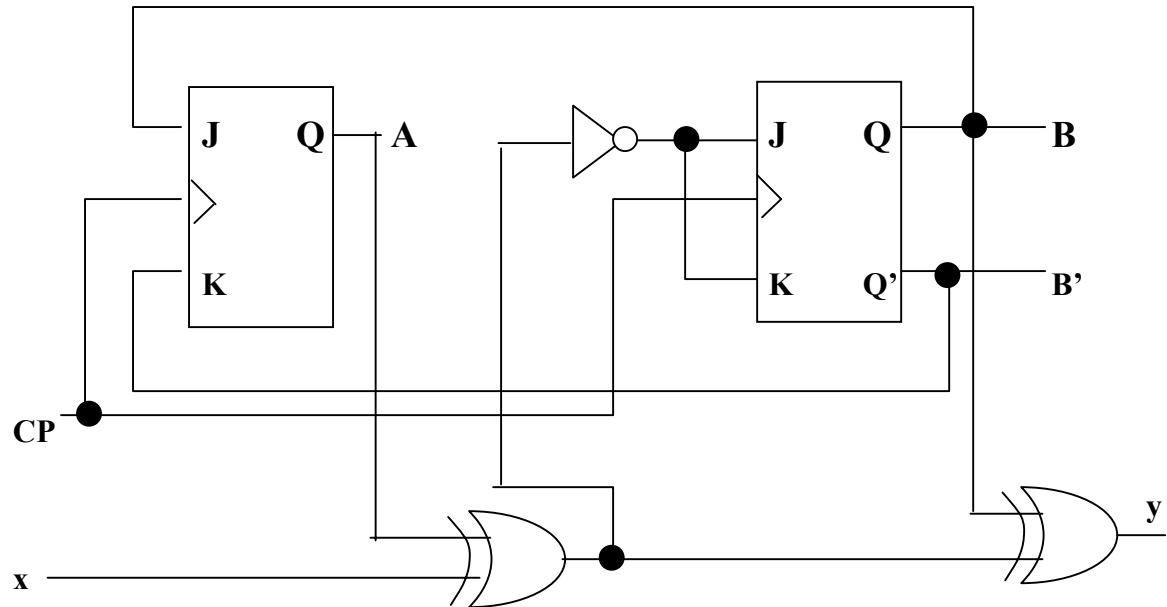


**Figure 2**

**Experimental Part :**

1. Implement your circuit in Preliminary Part 1 design in computer and test it's A,B,C flip-flops' outs -Q's- and the x:input and y:output in red probes.
2. Design and implementation of the sequential circuit with respect to the state diagram given in class from your laboratory instructor.