

Başkent University
Department of Electrical and Electronics Engineering
EEM 311 Electronics II
Experiment III

Single Stage MOSFET Amplifier

Aim:

The aim the experiment is to investigate the single stage MOSFET amplifier.

Theory :

The common-source amplifier with a NMOS transistor is shown in Figure 1. The input and output voltage signals are coupled to and from the amplifier with the use of coupling capacitors. The biasing is done by fixing the gate voltage with a voltage divider and also by using a source resistor R_S . The source resistor gives negative feedback and stabilizes the bias current as a function of temperature variations and transistor characteristics.

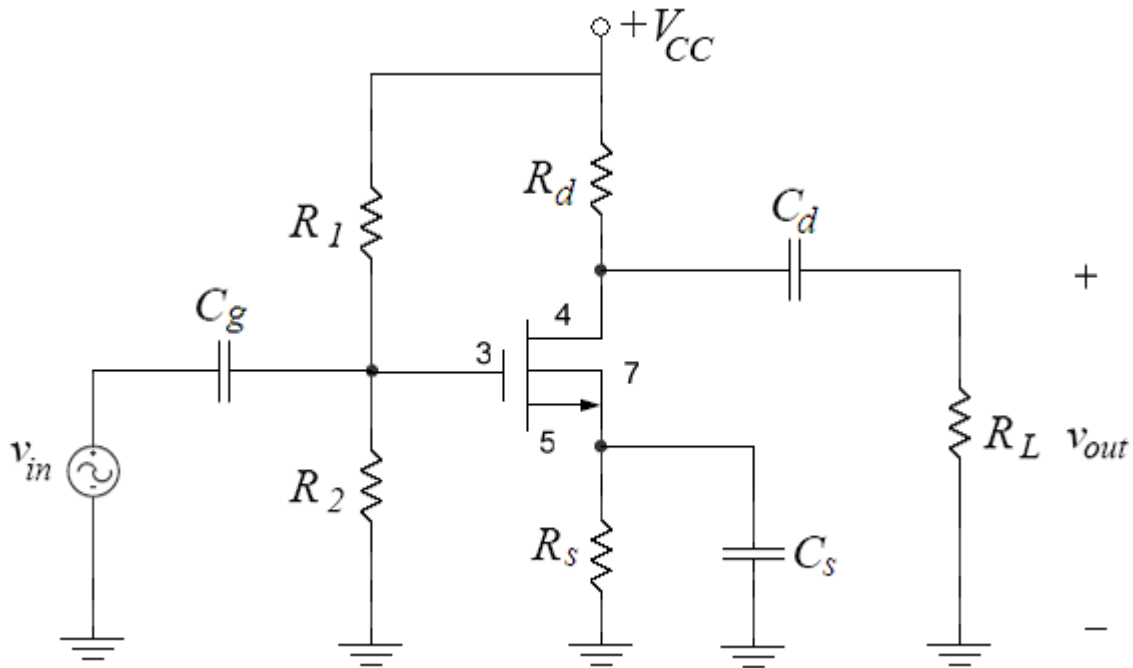


figure1

The small-signal model for MOSFET is shown in the Fig.2.

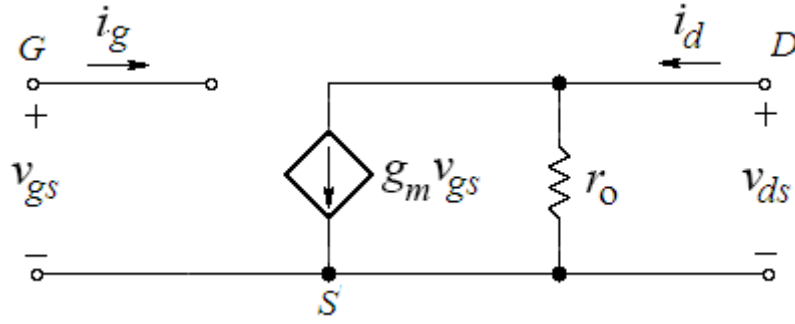


figure2

One of the most important characteristics of a transistor is its **transconductance** g_m that is a measure of how much the output current will vary when its input voltage v_{gs} changes. The transconductance g_m can be written as follows,

$$g_m = \frac{\partial i_D}{\partial v_{GS}} = k_n' \frac{W}{L} (V_{GS} - V_t) = \sqrt{2I_D k_n' \frac{W}{L}} = \frac{2I_D}{V_{GS} - V_t}$$

Thus the value of the transconductance depends on the bias current I_D .

The **small signal output resistor** of the MOSFET r_o is given by the ratio of the Early voltage $V_A=1/\lambda$ over the bias current,

$$r_o = \frac{V_A}{I_D} = \frac{1}{\lambda I_D}$$

The **amplification factor** of the MOSFET μ_f is also the product of g_m and r_o ;

$$\mu_f = g_m r_o = \frac{1}{\lambda I_D} \frac{2I_D}{V_{GS} - V_t} = \frac{2}{\lambda (V_{GS} - V_t)} = \frac{1}{\lambda} \sqrt{\frac{2k_n}{I_D}}$$

The amplification factor of the MOSFET decreases as the operating current increases.

Voltage Gain

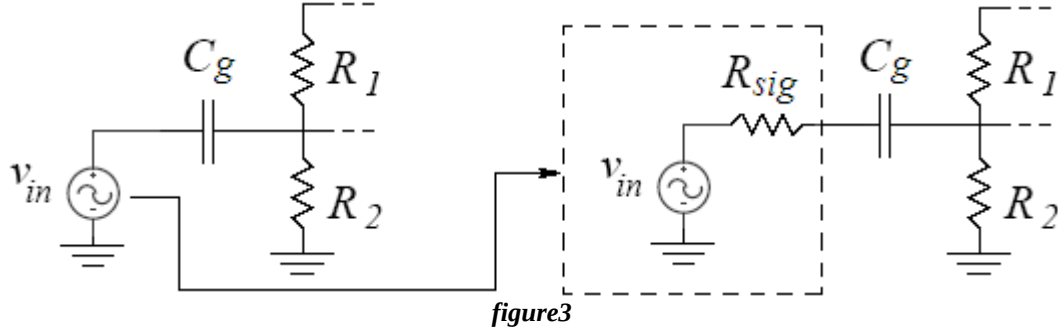
The overall voltage gain of the common source amplifier in Fig.1 is ;

$$A_v = \frac{v_{out}}{v_{in}} = -g_m (R_D \parallel R_L \parallel r_o)$$

In case the signal source has an internal resistance R_{sig} as shown in Fig.3(not shown in Fig.1), the value of the overall amplification will become,

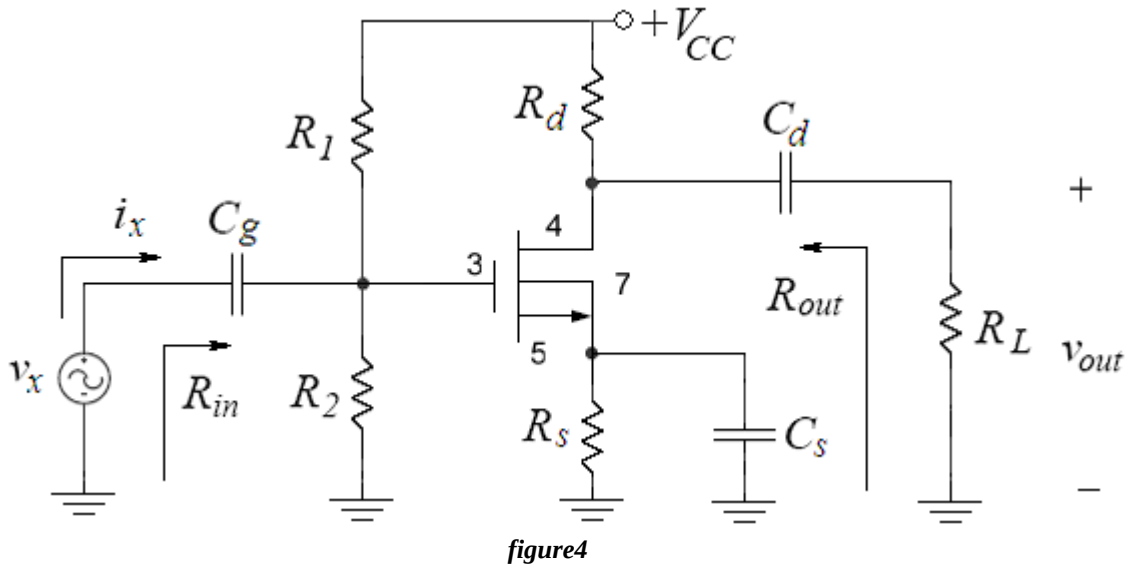
$$A_v = \frac{v_{out}}{v_{in}} = -\frac{R_G}{R_G + R_{sig}} g_m (R_D \parallel R_L \parallel r_o)$$

Notice that the internal resistance forms a voltage divider with the resistance $R_G = R_1 \parallel R_2$ which attenuates the input signal. It is for that reason that we need to keep the parallel resistance $R_1 \parallel R_2$ large as compare to R_{sig}



Input & Output Impedances

By hand calculations, the impedances are usually found by setting up either a test voltage source and finding the resulting input current into a point of interest, or by setting up a test current and finding the resultant voltage at the point of interest. The following figure is a display of the first method, setting up a test voltage v_x and test input current i_x and finding $R_{in} = v_x / i_x$;



For an amplifier like in Fig.4 before finding input impedance; the capacitors are considered to have zero impedance, the DC supplies are considered as an AC ground and transistors are replaced by its small signal model. This same approach can be applied to the output. It is important when solving for the output impedance that the point where the input source was connected to the original amplifier circuit be set as an AC ground point.

The input impedance of the amplifier in Fig.1 is equal to $R_{in} = R_G = R_1 \parallel R_2$ and the output impedance $R_{out} = R_D \parallel r_o$. For a voltage amplifier one likes to keep the input impedance large and the output impedance small. For the common-source amplifier, the input impedance is large. However, the output impedance is also large. It is for this reason that by adding a load resistor R_L at the output thus output impedance becomes $R_{out} = R_D \parallel r_o$, the output voltage and thus the amplification reduces. In order to obtain a small output

impedance, one can add a common-drain (or source follower) configuration after the common-source amplifier.

Knowledge:

Based upon the current technology in use, most MOSFET amplifiers are fabricated on integrated circuits. This fabrication process, with such small feature processing, makes it very difficult to create resistors on an integrated circuit. When fabricated, the resistors often have very undesirable tolerance values than can be as high as 10-20%, such that a large variation of resistance values results. This makes design very difficult. In this experiment, resistors will be used to perform the biasing of the MOSFET and to set the amplification. It is important to note that, because of the aforementioned fact, resistors are not used to bias and set amplification in modern MOSFET technology. Instead, MOSFET devices themselves are used as resistors that we know from the first electronic course and used to set bias conditions. These devices are made as was discovered in the MOSFET Transistor Basics experiments, which is similar to this experiment. So, try to discover something ☺☺☺.

Preliminary Work:

Review the sections 13.7, 13.8, 13.9, 13.10.2, 13.10.4 from the Course Book.

In preliminary work you will design single stage MOSFET amplifier, which has the circuit topology in Fig.1, using the one of the NMOS in CD4007C Chip. The Pin Diagram of the CD4007 Chip is in Fig.5. The DC supply voltage, the load resistance, and the coupling and bypass capacitor capacitances are given as:

V_{CC}	R_L	C_g	C_d	C_s
15 V	10 k Ω	1 μ F	1 μ F	10 μ F

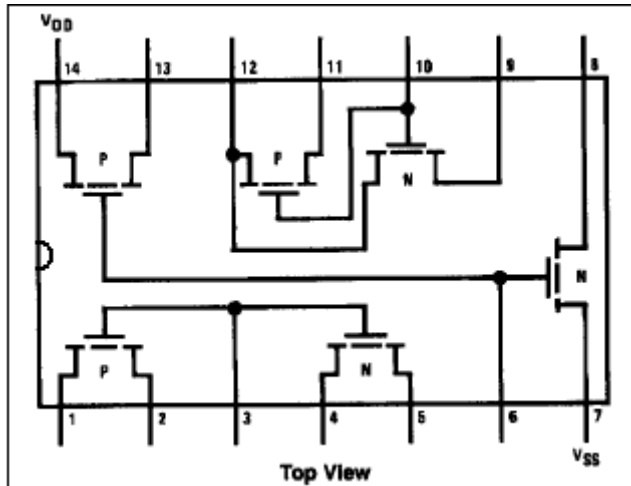


figure5

Reference:

[1] The values given for the $\mu_0 C_{ox}(W/L)$ and V_T found using the measured data on the CD4007 chip by Dr. David M. Binkley, Associate Professor at the University of North Carolina at Charlotte and Clark Hopper M.S, R.A. and Harold Hearne M.S., R. A. both also at the University of North Carolina at Charlotte.

The NMOS has $\mu_0 C_{ox} = 166.67 \mu A/V^2$, $W/L=3$ and $V_T = 1.45V$. Assume $V_A = 100V$.). (You can download data sheet [CD4007C.pdf](#) from course web page).

For the circuit shown in Fig.1, find values for R_1 , R_2 , R_D , and R_S such that the MOSFET is biased with an I_{DS} of approximately $75\mu\text{A}$, a V_{GS} of 2V , a V_D value to allow for maximum signal swing, and a V_S value to allow for the given bias conditions. Make sure the MOSFET is in saturation. (**Hint:** (Use only [Standard Resistor Values](#) less than or equal to $100\text{k}\Omega$. Make sure to allow for proper signal swing by adjusting V_S appropriately.)

1. For the circuit of Fig.1, use the values for R_1 , R_2 , R_D , and R_S . For signal frequencies of interest we can assume that the capacitors act as a short circuit.

- a. Draw the small signal AC equivalent of the circuit in Fig.1.
- b. Calculate the value of the transconductance g_m , small signal output resistor r_o and amplification factor μ_f .
- c. Find the voltage gain $A_v = v_{out}/v_{in}$.
- d. Find the input impedance R_{in} , and the output impedance R_{out} with the method described at the theory part (**Hint:** Use the small signal AC equivalent circuit).
- e. Calculate the largest value of the v_{in} that does not violate the small signal assumption. Calculate the peak-to-peak maximum undistorted voltage swing at the output.
- f. Calculate the peak-to-peak maximum (**unclipped**) voltage swing at the output.

Verify your design using PSpice. You will need to use a model for the CD4007 transistor. The models can be found in the CD4007.LIB library which you have it in **deney3.zip**. Save both the cd4007.lib and cd4007.olb_files in your directory. The transistors are called nnmos for the NMOS and pmos for the PMOS. You will need to add this library when drawing the schematic. Also, when creating a new Simulation Profile, while doing the simulation, you will need to add the library path and Filename (under the Libraries tab). See [PSpiceDocument.pdf](#), section 4 on "Using and Adding Vendor Libraries" or the **how to add an include file.doc** which you have it in **deney3.zip**.

- a. Form your circuit in Fig.1 in Pspice without the load resistor R_L and coupling capacitor C_d . For the transistor you need to add the CD4007 Library.
- b. Bias simulation. Simulate the circuit of Figure 1 (without the load resistor R_L). Do a BIAS simulation and find the **DC voltages at each node and current I_D** . Compare the results with the one you calculated in preliminary work part1.
- c. Next, do a transient simulation. Use as input signal a sinusoidal source (VSIN) of 1 kHz frequency and amplitude of 50mV . Do this first without a load resistor and next with a load R_L of $10\text{ k}\Omega$. Find the **input and output voltage**. What is the **voltage gain** with R_L and without R_L ? Compare the simulation results with your hand calculations.

- d. Summarize the **simulation results in table form** and hand it in together with the calculations and the **simulation print-outs**. Label each graph clearly.

Experimental Work:

You will be using the CD4007 MOSFET array for this experiment. This array contains three NMOS and three PMOS transistors as shown in Fig.5. Again, the key point to remember is that the bulk (or substrates) of all NMOS transistors are connected to the VSS (pin 7) and all PMOS substrates are connected to VDD (pin 14). When using this array pin 7 should be connected to the most negative supply voltage or to the source of the transistor. Pin 14 is the substrate of the PMOS and must be connected to the most positive supply voltage in the circuit!

The CD4007 MOSFET array should not be connected to circuits with the power on because high transient voltages may cause permanent damage. Therefore, **do not apply input signals until you have connected PIN 7 and 14; otherwise, serious damage to the device could result.**

You should note that the transistor characteristics of the CD4007 could vary considerably from chip to chip. The transistors may come from a different batch, what can explain why the threshold voltage, the transconductance parameter and the output resistance is different from the one used in the hand calculations and Spice simulation.

Precaution: MOSFET transistors are very susceptible to breakdown due to electrostatic discharge. It is recommended that you always ground yourself before picking up the MOSFET chip. Do not touch any of the pins of the chip.

Note: Use jumper wires as possible as short on your board to connect the pins of the transistors.

Before constructing the circuit,

- Verify the values of the resistors that you are going to use by measuring their resistances with a multimeter. Make sure that all resistors are within 2% of their marked values. This will assure that your current measurements are accurate
- Prepare the power supply for V_{CC} to ensure a DC voltage of 15V and adjust the function generator for v_{in} to a voltage level of approximately 50mVp-p at a frequency of 1kHz.

Construct the amplifier circuit using the values for the resistors R_1 , R_2 , R_d and R_s calculated in the preliminary work section and the values for R_L , C_g , C_d , C_s indicated in the preliminary work section.

Note: Always turn on the DC power supply before applying the AC signal. Always turn off the AC signal before turning off the DC power supply.

1. Measure and record V_G , V_D and V_S compare these with your calculations. Using the measured bias voltages V_G , V_D and V_S calculate the bias current I_{DS} . Compare these values with those calculated in the Preliminary work.

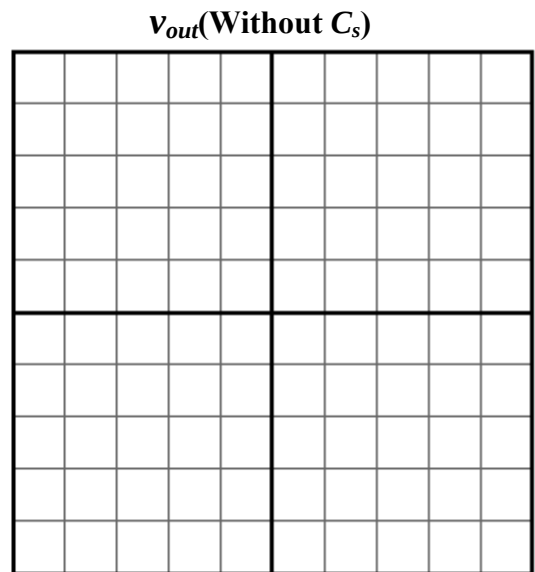
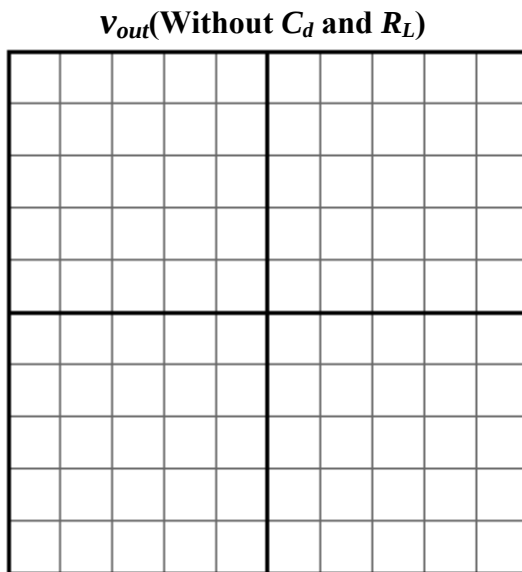
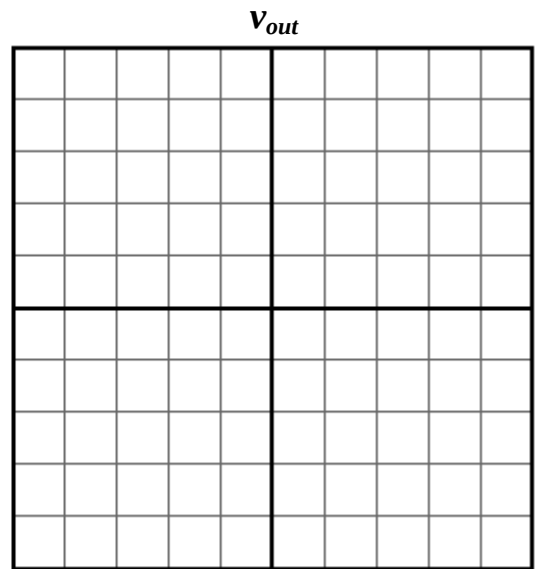
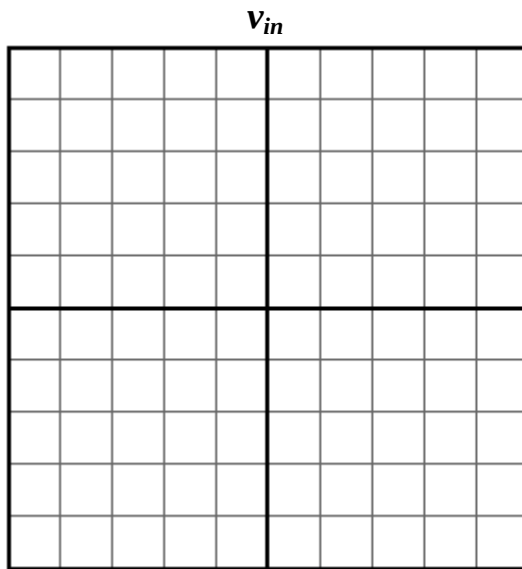
$$V_G =$$

$$V_D =$$

$$V_S =$$

2.

- a. Measure the voltage gain of your amplifier: Observe the input and output voltage waveforms on the oscilloscope. Calculate the voltage gain of the amplifier and compare with your calculations.
- b. Remove the capacitor C_d and load resistor R_L . Measure the output voltage v_{out} and the corresponding voltage gain(open circuit voltage gain) A_v . Notice that the DC voltage has added to the output voltage. What happened to the voltage gain? For your report, include a brief discussion on the effect of R_L .
- c. Add the coupling capacitor C_d and the load resistor R_L to the circuit and remove the bypass capacitor C_S over the source resistor. Measure the output signal. What is the voltage gain? Notice the strong effect of removing the capacitor on the amplification.



$$A_v =$$

$$A_{v,open\ circuit} =$$

$$A_{v, \text{without } C_s} =$$

3. Reconstruct the amplifier in Fig.1. Increase the amplitude of the input signal and observe the output signal. When does the output signal start to distort? What is the maximum output voltage swing before considerable distortion occurs?

$$V_{out, \text{maximum}} =$$

4. Measure the input impedance R_{in} . To do this, use the setup shown in the circuit diagram in Fig.6. Use the original input signal from the function generator ($v_x=50\text{mVp-p}$ @ 1kHz). Measure the value of v_{in} . Set up an equation relating v_x and v_{in} . Use that equation to solve for the value of the AC input impedance R_{in} .

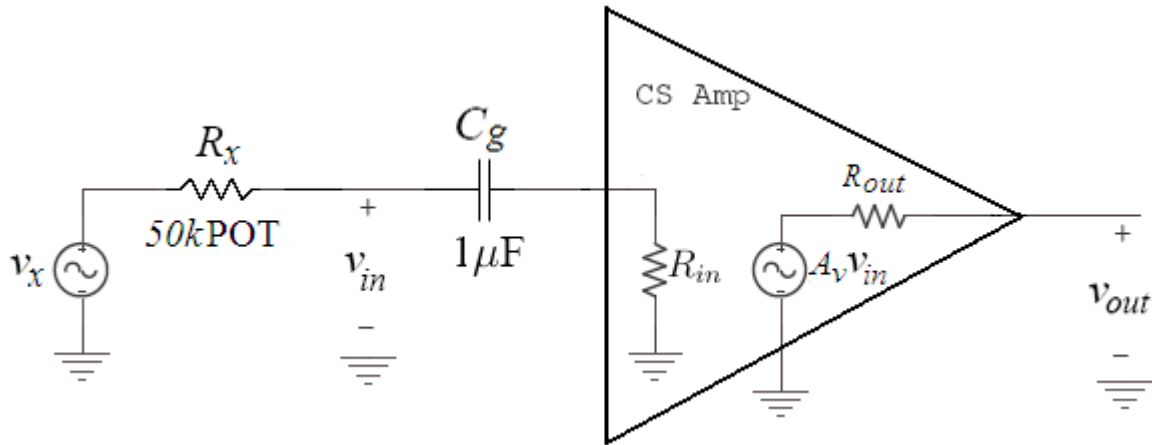


Figure6

$$v_{in} =$$

5. Measure the output impedance R_{out} . To do this, use the setup shown in the circuit diagram in Fig.7. Use the same input signal from the function generator ($v_x=50\text{mVp-p}$ @ 1kHz). Measure the value of v_{out} . Set up an equation relating v_{out} and v_x . Use that equation to solve for the value of the AC output impedance R_{out} . Make sure that R_L is not connected for this measurement!

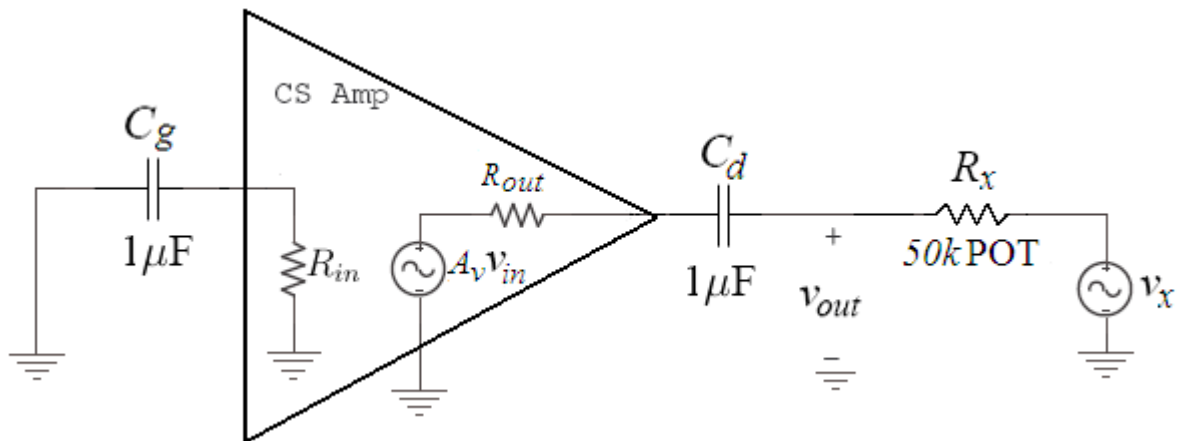


Figure7

$$V_{out} =$$

6. Compare the input impedance, and output impedance at 1kHz with that obtained in the Preliminary work.

Experiment Instruments:	Experiment Components:
- Breadboard - Oscilloscope - Signal Generator - Multimeter - DC Power Source	1 CD4007C Chip 1 10 k Ω 2 1 μ F 1 10 μ F 1 50kpot

Experiment Results

Part1	$V_G =$ $V_D =$ $V_S =$	
Part2	$A_v =$ $A_{v, open\ circuit} =$ $A_{v, without\ C_s} =$	
Part3	$V_{out, maximum} =$	
Part4	$V_{in} =$	
Part5	$V_{out} =$	

Student Name :

Signature.....