

Suppose we have connected the output of CMOS inverter 1 to the input of CMOS inverter 2, where the inverters have the following characteristics:

Both inverters:

$$\mu_N = 500 \text{ cm}^2 / (\text{Vs})$$

$$\mu_P = 250 \text{ cm}^2 / (\text{Vs})$$

$$V_{T(N)} = -V_{T(P)} = 1 \text{ V}$$

$$t_{ox} = 10 \text{ nm (oxide thickness)}$$

$$k_{ox} = 4 \text{ (oxide dielectric constant)}$$

$$V_{DD} = 5 \text{ V}$$

$$L_i = 20 \text{ } \mu\text{m (interconnect length)}$$

$$W_i = 1 \text{ } \mu\text{m (interconnect width)}$$

$$\epsilon_0 = 8.85 \times 10^{-12} \text{ F/m}$$

Inverter 1:

$$L_N = L_P = 2 \text{ } \mu\text{m}$$

$$W_N = 6 \text{ } \mu\text{m}$$

$$W_P = 24 \text{ } \mu\text{m}$$

$$C_{DB(P)} = C_{DB(N)} = 50 \text{ fF}$$

Inverter 2:

$$L_N = L_P = 2 \text{ } \mu\text{m}$$

$$W_N = 8 \text{ } \mu\text{m}$$

$$W_P = 16 \text{ } \mu\text{m}$$

$$C_{DB(P)} = C_{DB(N)} = 75 \text{ fF}$$

Find the propagation delay for the output of inverter 1, when the input of inverter 1 changes from logic 0 to logic 1 instantaneously (after being logic 0 for a long time).

$$t_p = 0.69 \tau$$

$$\tau = R_N (C_{DBN1} + C_{DBP1} + C_{GBN2} + C_{GBP2} + C_I)$$

$$R_N = 0.75 V_{DD} / I_{DSAT1} = 0.75 V_{DD} / \left(\frac{W_{N1}}{2 L_{N1}} \mu_N C_{ox} (V_{GS1} - V_T)^2 \right)$$

$$= 0.75(5) / \left[\left(\frac{6 \cdot 10^{-6}}{2 \cdot 2 \cdot 10^{-9}} \right) (500 \cdot 10^{-4}) \left(\frac{4(8.85 \cdot 10^{-12})}{10 \cdot 10^{-9}} \right) (5-1)^2 \right]$$

$$= 883 \Omega$$

$$C_{GBN2} = C_{ox} W_{N2} L_{N2} = \frac{4(8.85 \cdot 10^{-12})}{10 \cdot 10^{-9}} (8 \cdot 10^{-6}) (2 \cdot 10^{-6}) = 56 \text{ fF}$$

$$C_{GBP2} = C_{ox} W_{P2} L_{P2} = \frac{4(8.85 \cdot 10^{-12})}{10 \cdot 10^{-9}} (16 \cdot 10^{-6}) (2 \cdot 10^{-6}) = 112 \text{ fF}$$

$$C_I = C_{ox} W_i L_i = \frac{4(8.85 \cdot 10^{-12})}{10 \cdot 10^{-9}} (1 \cdot 10^{-6}) (20 \cdot 10^{-6}) = 70 \text{ fF}$$

$$t_p = 0.69 (883) (56 + 112 + 70 + 50 + 50) 10^{-15}$$

$$= 206 \text{ pS}$$

Suppose I hook an inverter up to one of the inputs of our 3-bit adder's most significant digit function. Find the propagation delay from the input to the output of the inverter when the inverter input A goes from low to high (with the other adder inputs held constant as shown).

For all of the gates, use

$$C_{DB(P)} = C_{DB(N)} = 50 \text{ fF}$$

$$C_{GB(P)} = 50 \text{ fF}$$

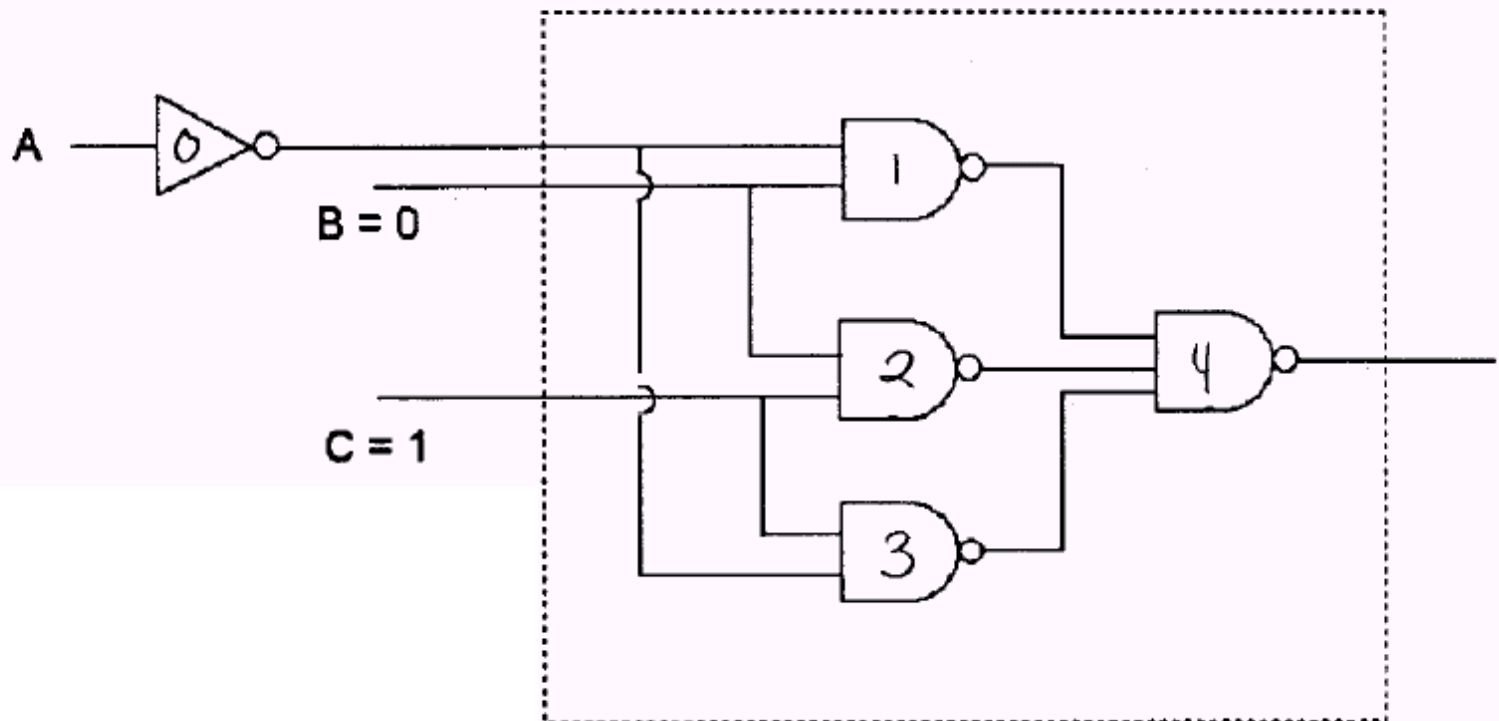
$$C_{GB(N)} = 75 \text{ fF}$$

$$C_I = 100 \text{ fF per gate}$$

$$R_N = 3 \text{ k}\Omega$$

$$R_P = 2 \text{ k}\Omega$$

A NAND-NAND implementation of the circuit is shown below.



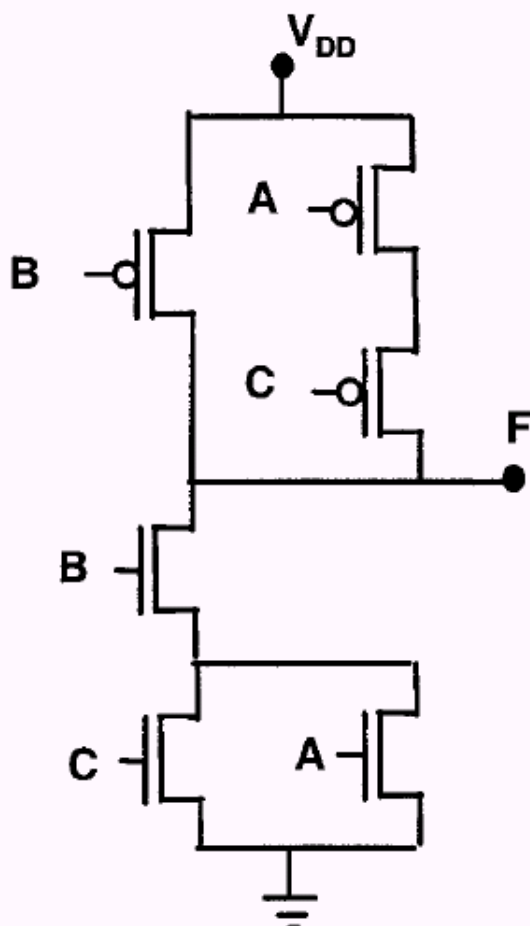
Gates 1 and 3
affect delay thru
the inverter (others
not directly attached)

One connection to gate 1 and one connection to gate 3:
Use 2 gate capacitances (C_{GBN} and C_{GBP}) for gate 1 and
for gate 3. Use 2 C_I (2 gates connected).

$$\begin{aligned} t_p &= 0.69 R_N (C_{DBN_0} + C_{DBP_0} + C_{GBN_1} + C_{GBP_1} + C_{GBN_3} + C_{GBP_3} + 2C_I) \\ &= 0.69 (3000) (50 + 50 + 75 + 50 + 75 + 50 + 2 \cdot 100) 10^{-15} \\ &= 1.14 \text{ ns} \end{aligned}$$

Determine whether the circuit below performs a logical operation. If it does, give the Boolean function it computes. If not, give a set of inputs that results in an invalid output.

For your convenience, 8 copies of this circuit are given on the next page. Assume that all PMOS transistors have source terminal on top, and all NMOS transistors have source terminal on the bottom.



From looking at PMOS half: $F = V_{DD}$ if
B conducts OR (A conducts AND C conducts)

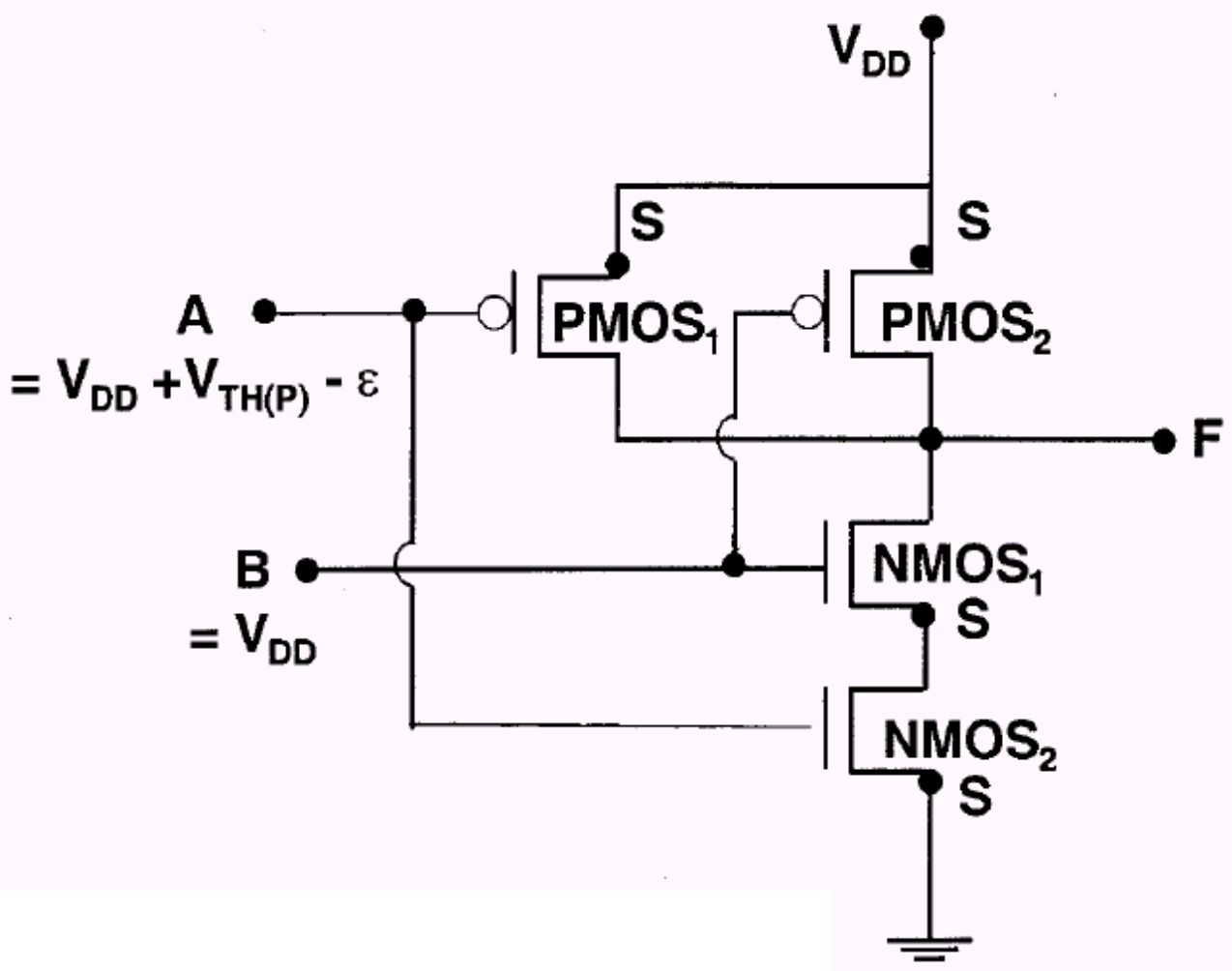
$$F = \overline{B} + \overline{A} \overline{C}$$

From looking at NMOS half: $F = 0$ if
B conducts AND (A conducts OR C conducts)

$$\overline{F} = B(A + C)$$

These agree by De Morgan's law; it is a logic circuit

For the CMOS logic circuit below, determine the most probable mode of operation for each transistor. Assume that ϵ is a very small positive number, and V_{DD} is much larger in magnitude than either V_{TH} .



PMOS₂ cutoff ($V_{GSP2} = V_{DD} - V_{DD} = 0V$)

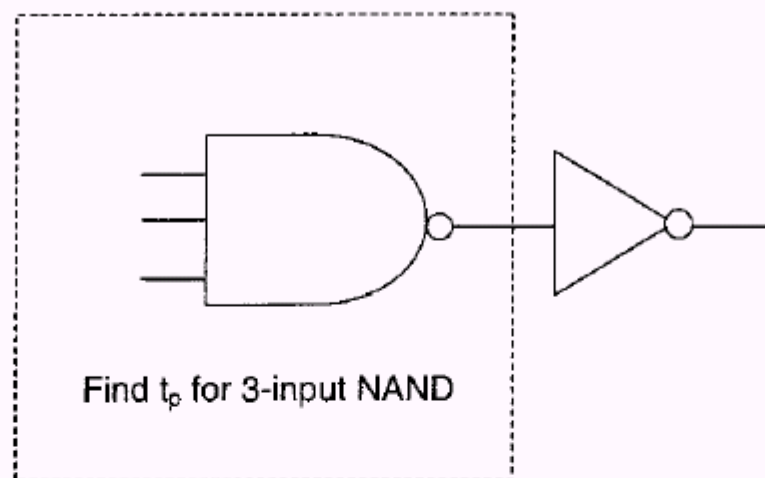
PMOS₁ barely on ($V_{GSP1} = V_{DD} + V_{THP} - \epsilon - V_{DD} = V_{THP} - \epsilon$)

I_D shared by PMOS₁, NMOS₁, NMOS₂ is small

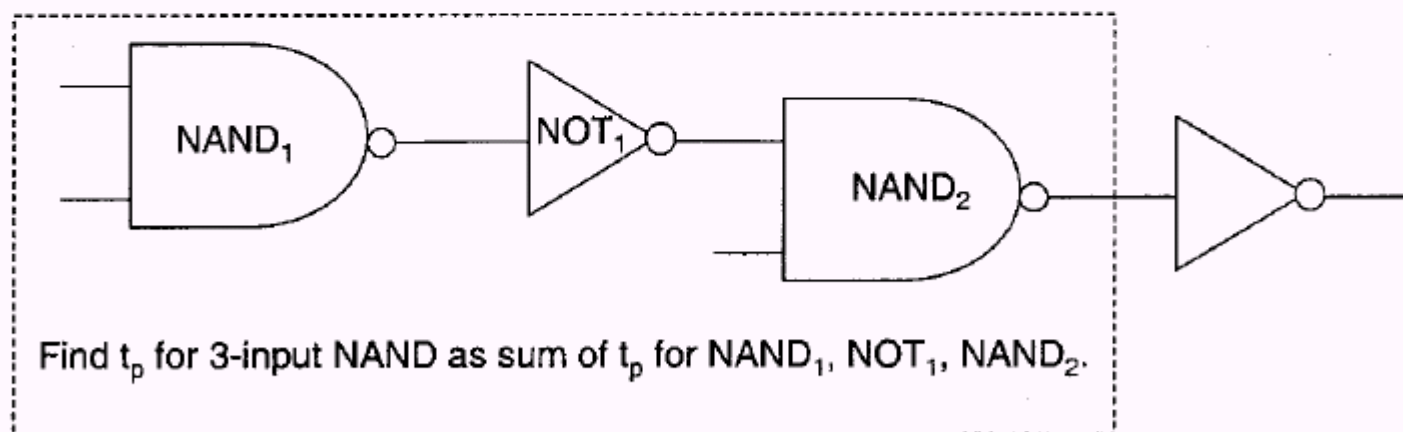
$V_{GSN2} = V_{DD} + V_{THP} - \epsilon$ for NMOS₂ is not small and is positive, since V_{DD} is much larger in magnitude than V_{THP} or ϵ (by assumption).

NMOS₁ on with small $I_D \Rightarrow$ NMOS₂ triode

Find the propagation delay for this 3-input NAND gate with inverter load,



where the 3-input NAND is implemented using two 2-input NAND gates and an inverter:



Compute the propagation delay t_p for the 3-input NAND as the sum of the worst-case propagation delays of the individual gates inside.

Use $R_N = 1\text{ k}\Omega$, $R_P = 2\text{ k}\Omega$, and $C_G = 10\text{ fF}$ per transistor. Ignore interconnect capacitance.

$$\text{NAND}_1: t_p = 0.69 R_p (2C_G) = 27.6 \text{ ps}$$



Same for NAND_2 .

Worst-case resistance is $2R_N$ or R_P (equal)

$C_{out} = 2C_G$
(inverter has 2 transistors)

$$\text{NOT}_1: t_p = 0.69 R_p (2C_G) = 27.6 \text{ ps}$$



Total t_p for 3-input NAND: $3(27.6 \text{ ps}) = 82.8 \text{ ps}$

Worst-case resistance is R_P .

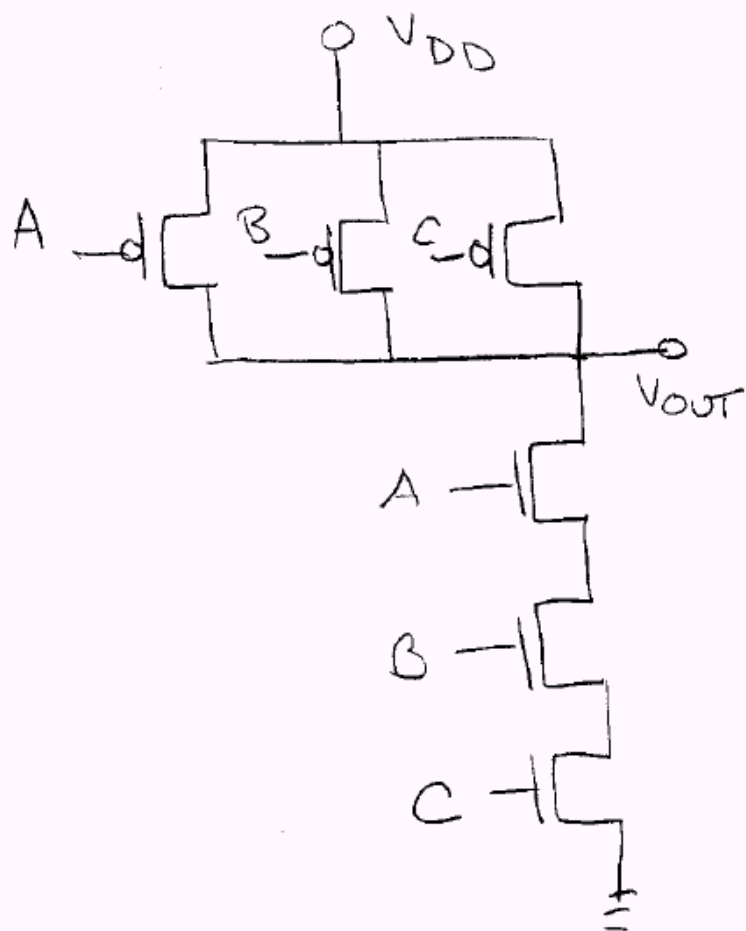
$C_{out} = 2C_G$
(output goes to one input of NAND: 2 of the 4 transistors)

Design a circuit, using only NMOS and PMOS transistors (and a power supply), that performs the 3-input NAND function with **shorter** worst-case propagation delay than the implementation given in Problem 5, when a single inverter is attached as the output load.

Assume that your transistors have the same characteristics as those in Problem 5:

Use $R_N = 1 \text{ k}\Omega$, $R_P = 2 \text{ k}\Omega$, and $C_G = 10 \text{ fF}$ per transistor. Ignore interconnect capacitance.

Provide your design and its worst-case propagation delay with single inverter output load.



Worst-case resistance:
 $3R_N$ (pull-down)

If attached to inverter,
 $C_{OUT} = 2C_G$

$$t_p = 0.69(3R_N)(2C_G) \\ = 41.4 \text{ ps}$$

(half the delay of
 the Problem 5 analysis)

- a) (4 pts) Find the final value of the voltage V_o , as a response to a LH transition at the input as shown in Figures 1.a – 1.d. Assume $V_{TN} = |V_{TP}| = 0.5V$. Assume that the capacitor is initially discharged, and ignore subthreshold conduction and body effect.

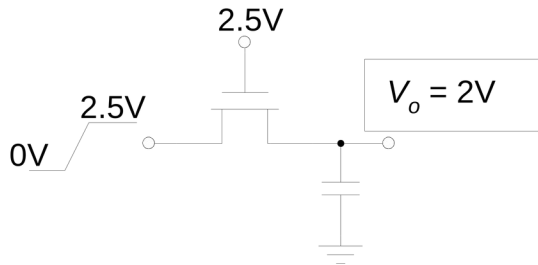


Figure 1.a.

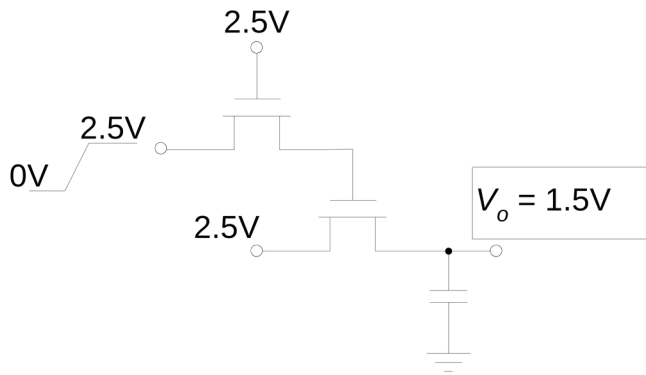


Figure 1.b.

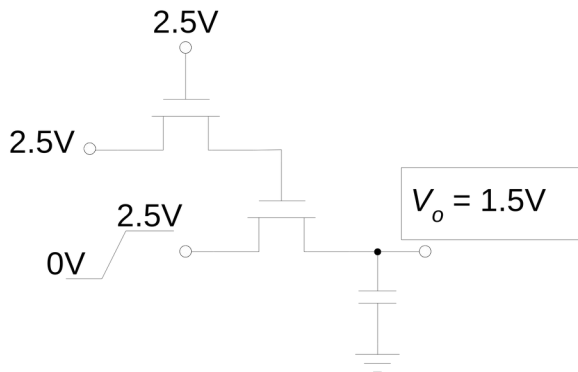


Figure 1.c.

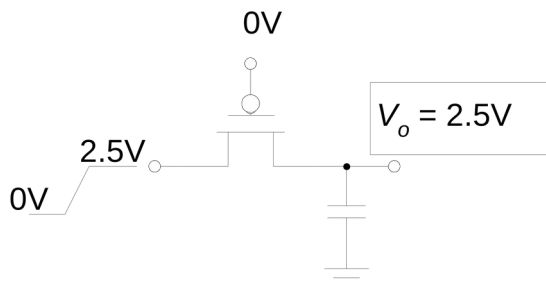


Figure 1.d.

b) (2pts) When the output reaches its final value, a 2.5V to 0 step is applied to the input. Determine the energy consumed in the transistors from Figure 1.c. during the transition (in symbolic terms).

$$E_{dis} = \frac{1}{2} C (V - 2V_T)^2$$

$$E_{1 \rightarrow 0} = \frac{1}{2} C (V - 2V_T)^2$$

c) (6pts) For Figure 1.d, find the energy dissipated in the transistor during the first 0 → 1 transition. Then, when the output reaches its final value, a 2.5V to 0 step is applied to the input, followed by the second 0 to 2.5V step. Find the energy dissipated in the transistor in the first 1 → 0 transition, and the second 0 → 1 transition (in symbolic terms).

$$\text{First } E_{0 \rightarrow 1} = \frac{1}{2} C V^2$$

$$\text{First } E_{1 \rightarrow 0} = \frac{1}{2} C (V^2 - V_T^2)$$

$$\text{Second } E_{0 \rightarrow 1} = \frac{1}{2} C (V - V_T)^2$$