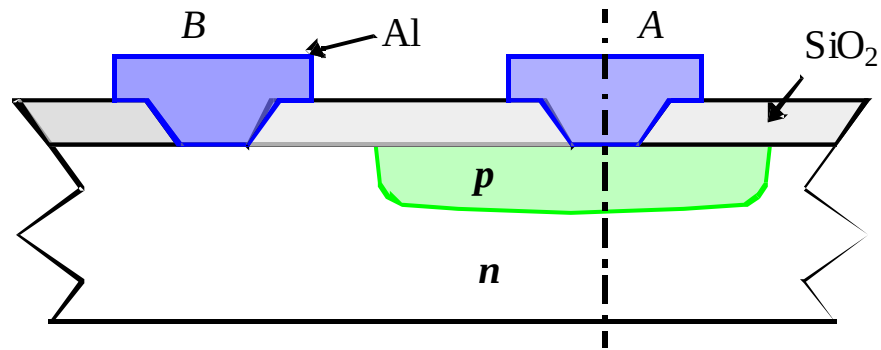
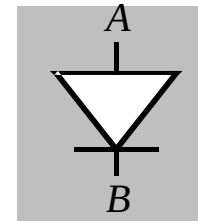
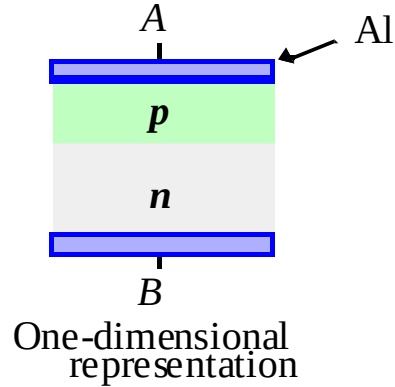


The Diode

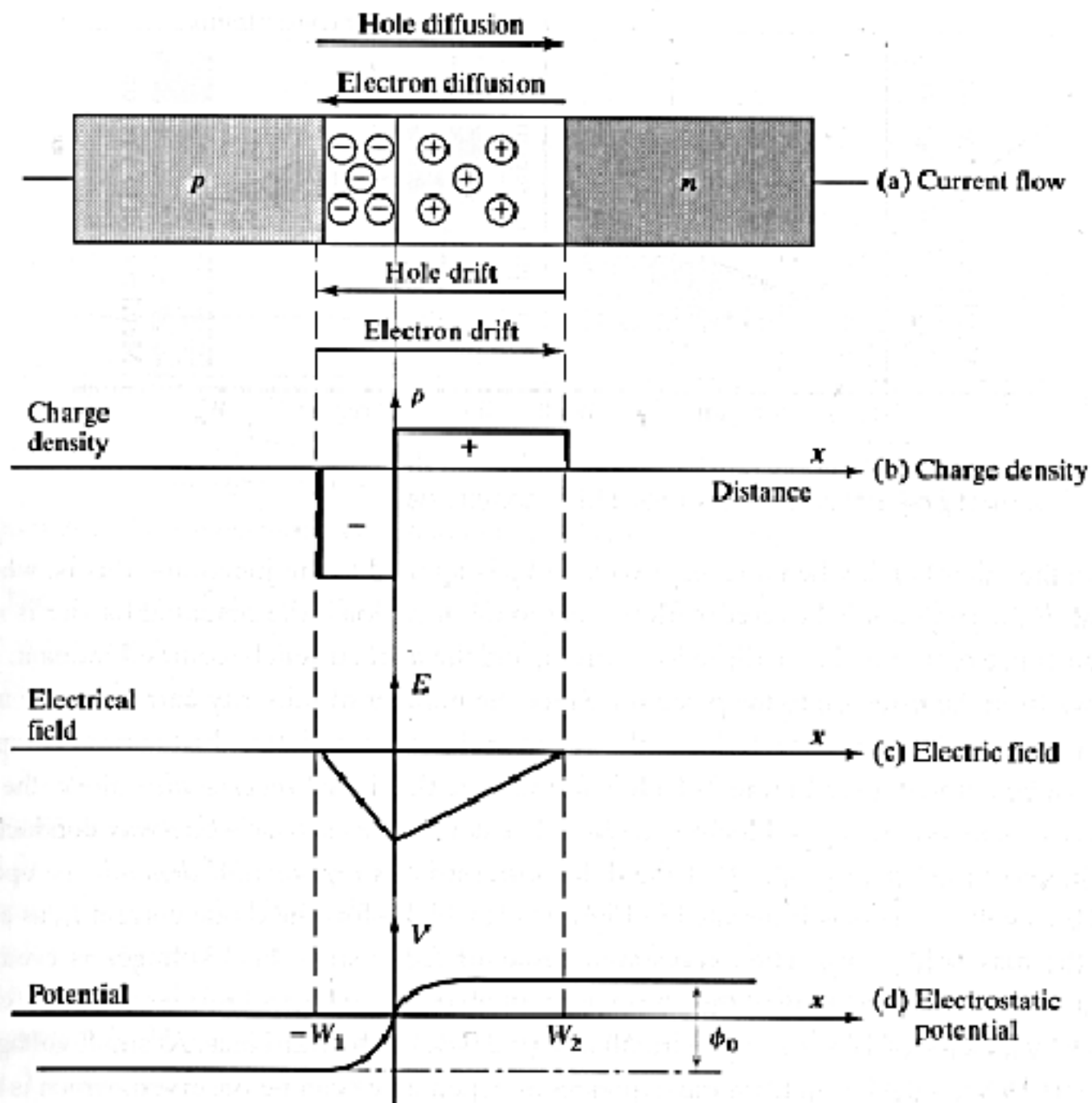


Cross-section of p - n junction in an IC process

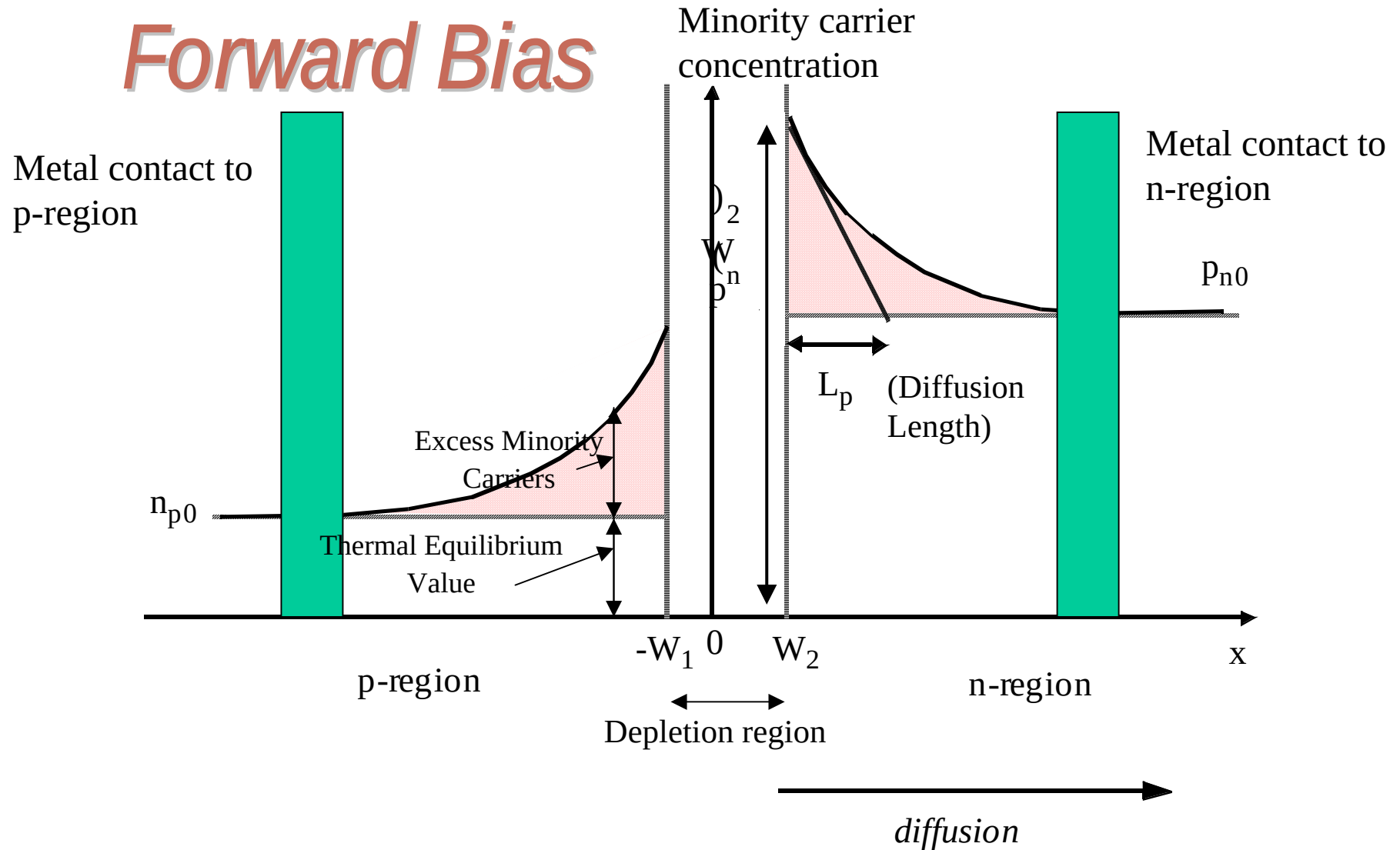


diode symbol

Mostly occurring as parasitic element in Digital ICs

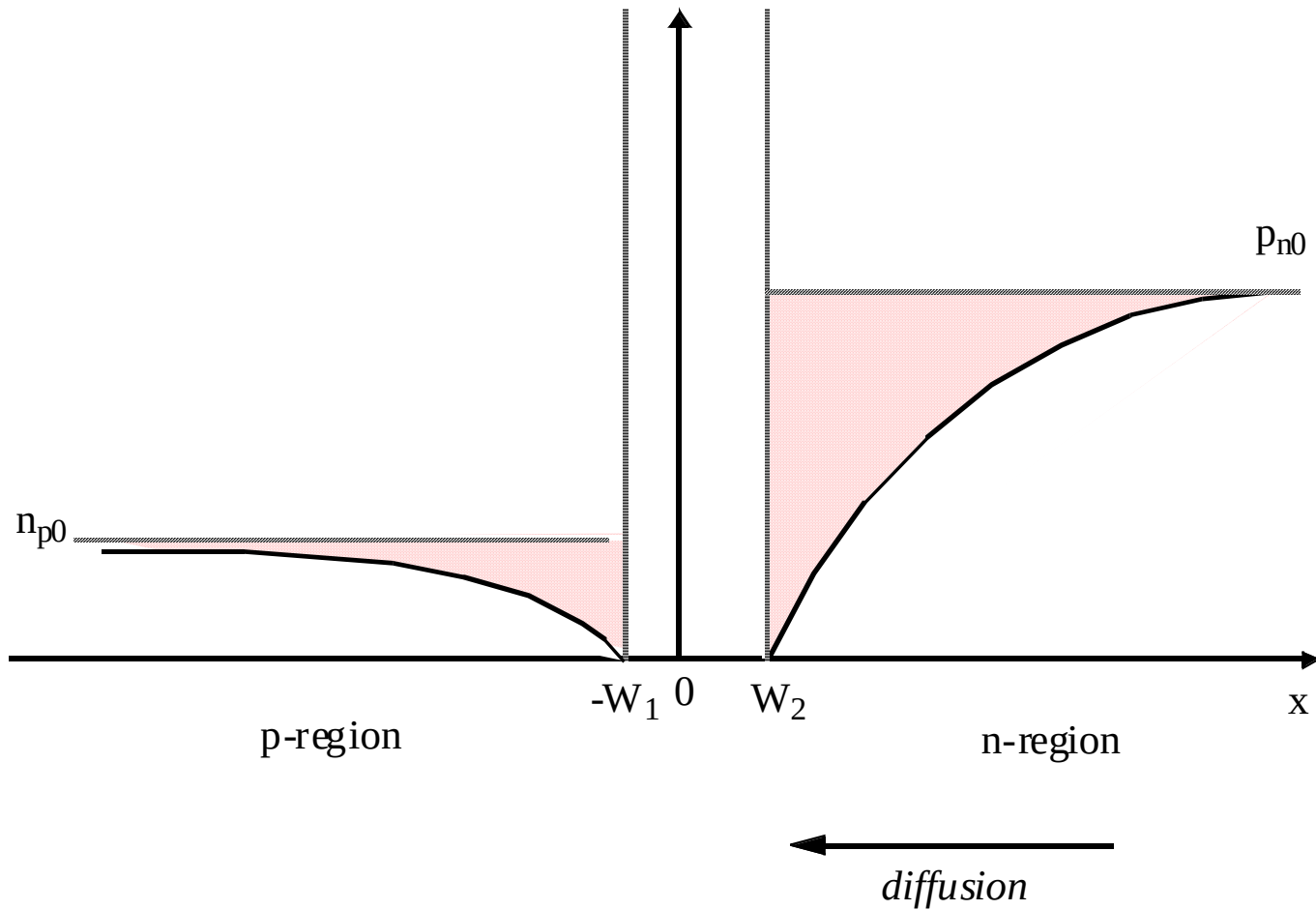


Forward Bias



Typically avoided in Digital ICs

Reverse Bias



The Dominant Operation Mode

$$I_D = I_S (e^{V_D/\Phi_T} - 1)$$

$$\text{Build-in potential} = \Phi_0 = \Phi_T \ln \left[\frac{N_A N_D}{n_i^2} \right]$$

$$\text{Thermal Voltage} = \Phi_T = \frac{kT}{q} = 26mV \quad \text{at } 300K$$

N_A = Acceptor concentration

N_D = Donor concentration

n_i = intrinsic carrier concentration $\cong 1.5 \times 10^{10} \text{ cm}^{-3}$
for silicon, at 300K

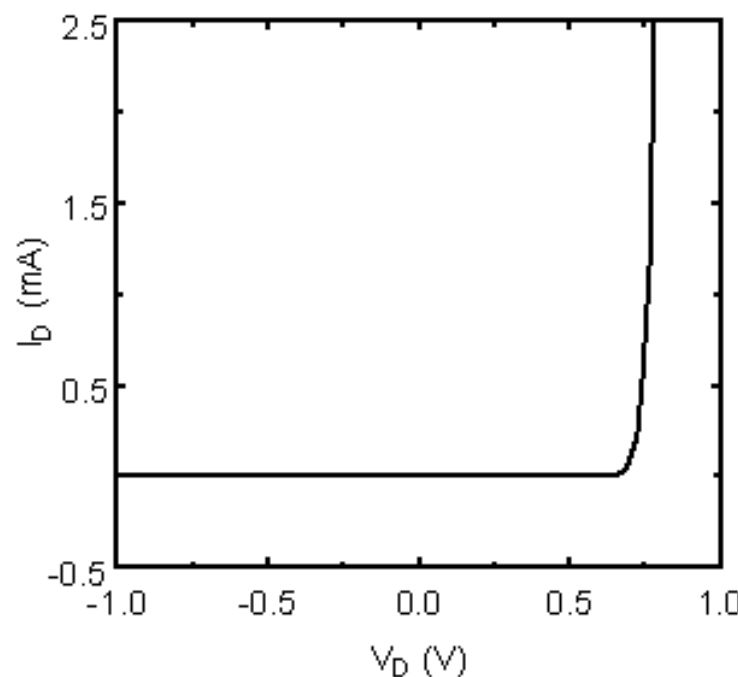
k = Boltzmann's constant = 1.38×10^{-23} joules/kelvin

T = Absolute temperature in kelvins = $273 + C^\circ$

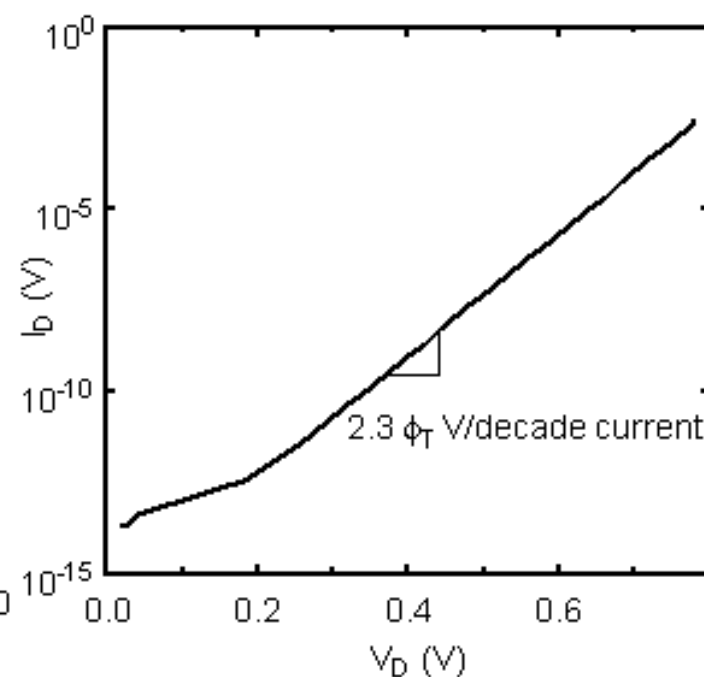
q = Electric charge = 1.6×10^{-19} coulomb

- I_S is usually called the saturation current and it is directly proportional to the cross-sectional area of the diode.
- The value of I_S is a very strong function of the temperature and it generally doubles for every 5°C rise in temperature.
- In actual devices, the reverse current is substantially (about 3 times) larger than I_S . That is due to the thermal generation of hole and electron pairs in the depletion region, which are swept out by the electric field, generating additional current component. Reverse current doubles for every 10°C in temperature.
- For typical silicon junctions, I_S is nominally in the range of 10^{-17} A/ μm^2
- ϕ_0 is also called the cut-in voltage (0.6 – 0.8V)

Diode Current



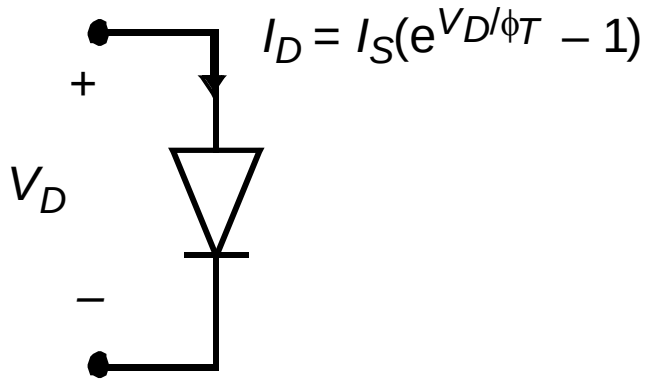
(a) On a linear scale.



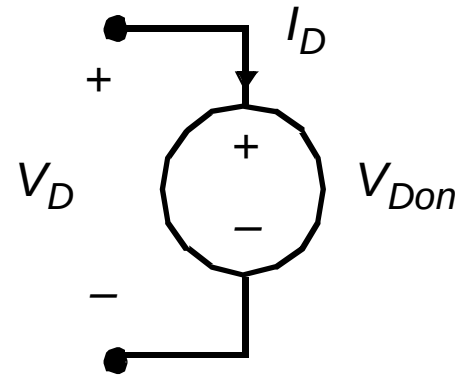
(b) On a logarithmic scale (forward bias).

$$I_D = I_S \left(e^{V_D / \phi_T} - 1 \right)$$

Models for Manual Analysis



(a) Ideal diode model



(b) First-order diode model

Consider the simple network of Figure 3-7 and assume that $V_S = 3 \text{ V}$, $R_S = 10 \text{ k}\Omega$, and $I_S = 0.5 \times 10^{-16} \text{ A}$. The diode current and voltage are related by the following network equation:

$$V_S - R_S I_D = V_D$$

Inserting the ideal diode equation and (painfully) solving the nonlinear equation using numerical or iterative techniques yields the following solution: $I_D = 0.224 \text{ mA}$, and $V_D = 0.757 \text{ V}$. The simplified model with $V_{Don} = 0.7 \text{ V}$ produces similar results ($V_D = 0.7 \text{ V}$, $I_D = 0.23 \text{ A}$) with far less effort. Hence, it makes considerable sense to use this model when determining a first-order solution of a diode network.

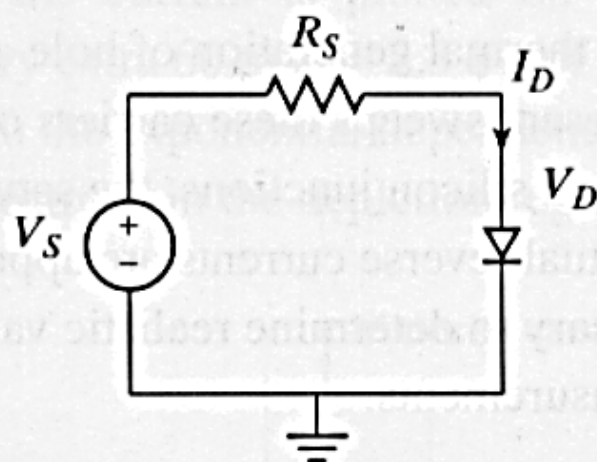


Figure 3-7 A simple diode circuit.

Depletion region charge:

Space charge is equal at both sides (p&n) of depletion region

$$-qW_1N_A A_D = qW_2N_D A_D \rightarrow -\frac{W_2}{W_1} = \frac{N_A}{N_D} \rightarrow W_1 = -W_2 \frac{N_D}{N_A} \dots\dots (1)$$

Depletion region width: $W_j = W_2 - W_1 \rightarrow W_2 = W_j + W_1 \dots\dots (2)$

Inserting (1) into (2) $\rightarrow W_2 = W_j - W_2 \frac{N_D}{N_A} \rightarrow W_2 \left(1 + \frac{N_D}{N_A} \right) = W_j$

$$W_2 = \frac{W_j}{1 + N_D / N_A} \dots\dots (3) \quad \text{Note that } W_1 \text{ is negative}$$

Depletion region charge: $Q_j \quad Q_j = Q_N = qW_2N_D A_D \dots\dots (4)$

Inserting (3) into (4) $\rightarrow Q_j = qN_D \frac{W_j A_D}{1 + N_D / N_A} = \frac{qN_D W_j A_D}{(N_A + N_D) / N_A}$

$$Q_j = q \frac{N_A N_D}{N_A + N_D} A_D W_j \dots\dots\dots (5)$$

Device physics state that: $W_j = \sqrt{\frac{2\epsilon_{si}}{q} \frac{N_A + N_D}{N_A N_D} (\Phi_0 - V_D)} \dots\dots\dots (6)$

Inserting (6) into (5) $\rightarrow Q_j = q \frac{N_A N_D}{N_A + N_D} A_D \sqrt{\frac{2\epsilon_{si}}{q} \frac{N_A + N_D}{N_A N_D} (\Phi_0 - V_D)}$

$$Q_j = A_D \sqrt{\frac{2\epsilon_{si} \cancel{q}^2}{\cancel{q}} \frac{(N_A N_D)^2}{(N_A + N_D)^2} \frac{\cancel{N_A + N_D}}{\cancel{N_A N_D}} (\Phi_0 - V_D)}$$

$$Q_j = A_D \sqrt{\left(2\epsilon_{si} q \frac{N_A N_D}{N_A + N_D} \right) (\Phi_0 - V_D)}$$

Note that, V_D is negative for reverse bias

Maximum electric field:

Gaussian Law: $\varepsilon_0 \Phi_E = \varepsilon_0 EA = q \rightarrow E = \frac{q}{\varepsilon_0 A}$

$$E_j = \frac{Q_j}{\varepsilon_{si} A_D} = \frac{\cancel{A_D} \sqrt{2\varepsilon_{si} q \frac{N_A N_D}{N_A + N_D} (\Phi_0 - V_D)}}{\varepsilon_{si} \cancel{A_D}}$$

$$E_j = \sqrt{\frac{2\varepsilon_{si} q \frac{N_A N_D}{N_A + N_D} (\Phi_0 - V_D)}{\varepsilon_{si}}} = \boxed{\sqrt{\frac{2q}{\varepsilon_{si}} \frac{N_A N_D}{N_A + N_D} (\Phi_0 - V_D)}}$$

Junction Capacitance:

Because the space charge region contains few mobile carriers, it acts as an insulator with a dielectric constant ϵ_{si}
n and p regions act as capacitor plates.

$$Q_j = A_D \sqrt{\left(2\epsilon_{si}q \frac{N_A N_D}{N_A + N_D}\right)(\Phi_0 - V_D)} = A_D \left[\left(2\epsilon_{si}q \frac{N_A N_D}{N_A + N_D}\right)(\Phi_0 - V_D) \right]^{1/2}$$

$$C_j = \frac{dQ_j}{dV_D} = A_D \frac{1}{2} \left(2\epsilon_{si}q \frac{N_A N_D}{N_A + N_D}\right) \left[\left(2\epsilon_{si}q \frac{N_A N_D}{N_A + N_D}\right)(\Phi_0 - V_D) \right]^{-1/2}$$
$$= \frac{A_D}{2} \frac{2\epsilon_{si}q \frac{N_A N_D}{N_A + N_D}}{\sqrt{\left(2\epsilon_{si}q \frac{N_A N_D}{N_A + N_D}\right)(\Phi_0 - V_D)}} = \frac{A_D}{2} \sqrt{\frac{\left(2\epsilon_{si}q \frac{N_A N_D}{N_A + N_D}\right)^2}{\left(2\epsilon_{si}q \frac{N_A N_D}{N_A + N_D}\right)(\Phi_0 - V_D)}}$$

$$= A_D \sqrt{\frac{1}{2} \frac{\cancel{2} \varepsilon_{si} q \frac{N_A N_D}{N_A + N_D}}{\Phi_0 - V_D}} = A_D \sqrt{\frac{1}{2} \varepsilon_{si} q \frac{N_A N_D}{N_A + N_D} (\Phi_0 - V_D)^{-1}}$$

let $C_{j0} = C_j$ when $V_D = 0$ (zero bias) $\rightarrow C_{j0} = A_D \sqrt{\frac{\varepsilon_{si} q}{2} \frac{N_A N_D}{N_A + N_D} \Phi_0^{-1}}$

$$C_j = A_D \sqrt{\frac{\frac{\varepsilon_{si} q}{2} \frac{N_A N_D}{N_A + N_D}}{\Phi_0 - V_D}} = A_D \sqrt{\frac{\frac{\varepsilon_{si} q}{2} \frac{N_A N_D}{N_A + N_D}}{\Phi_0}} \frac{\Phi_0}{\Phi_0 - V_D}$$

$$C_j = \frac{C_{j0}}{\sqrt{\frac{\Phi_0 - V_D}{\Phi_0}}}$$

$$\frac{\Phi_0 - V_D}{\Phi_0} = 1 - \frac{V_D}{\Phi_0}$$

$$C_j = \frac{C_{j0}}{\sqrt{1 - \frac{V_D}{\Phi_0}}}$$

Diffusion Capacitance

The dynamic behavior of the diode is modeled by the nonlinear capacitance C_D , which combines the charge storage effects of the space charge and the excess minority carriers.

$$Q = \text{excess minority carrier stored charge} = \tau_T I_D = \tau_T I_S (e^{V_D / n \Phi_T} - 1)$$

$$Q \cong \tau_T I_S e^{V_D / n \Phi_T} \text{ for } I_D \gg I_S$$

where n = emission coefficient = 1 for most diodes, and

τ_T is the mean transit time. Since $C_d = \frac{dQ}{dV_D}$ = diffusion capacitance,

$$C_D = C_j + C_d = \frac{C_{j0}}{(1 - V_D / \Phi_0)^m} + \frac{\tau_T I_S}{\Phi_T} e^{V_D / n \Phi_T}$$

C_d is significant under forward bias conditions, which is not a case in digital integrated circuits. Here, m is called the grading coefficient and it is equal to 1/2 for abrupt junctions.

1. Depletion region charge (V_D is negative for reverse bias):

$$Q_j = A_D \sqrt{\left(2\epsilon_{si} q \frac{N_A N_D}{N_A + N_D} \right) (\Phi_0 - V_D)}$$

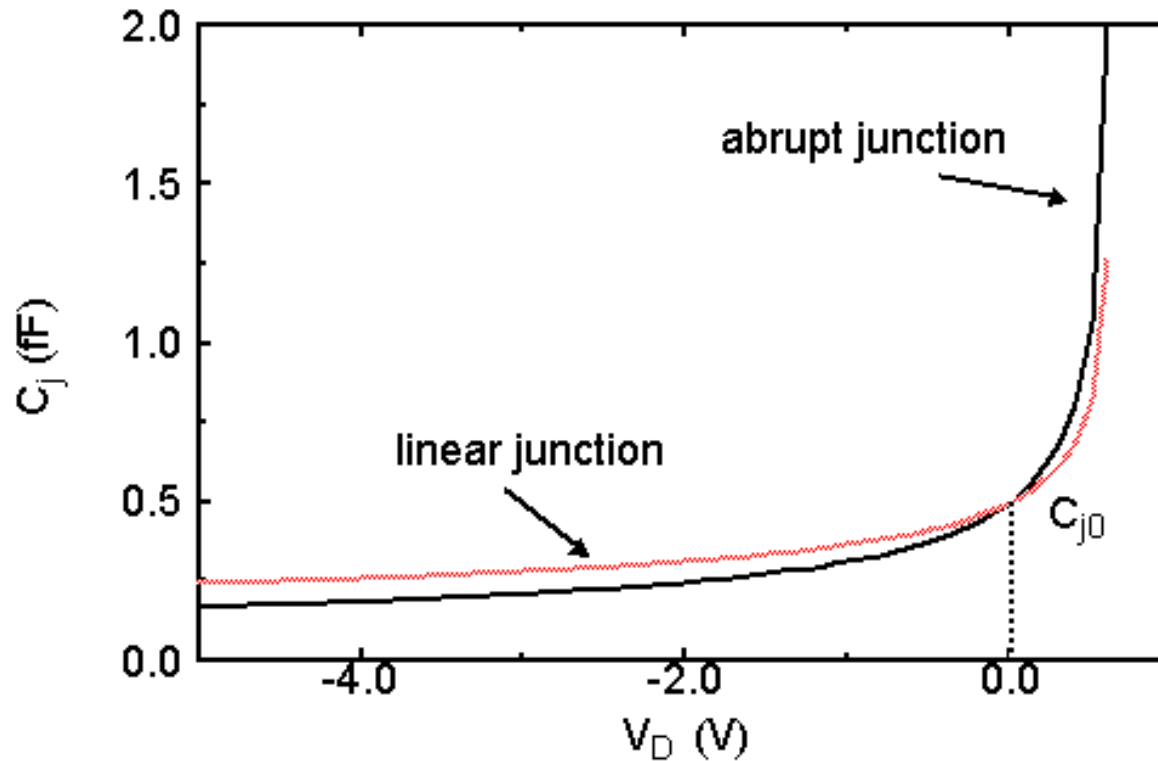
2. Depletion region width:

$$W_j = W_2 - W_1 = \sqrt{\frac{2\epsilon_{si}}{q} \frac{N_A + N_D}{N_A N_D} (\Phi_0 - V_D)}$$

3. Maximum electric field:

$$E_j = \sqrt{\left(\frac{2q}{\epsilon_{si}} \frac{N_A N_D}{N_A + N_D} \right) (\Phi_0 - V_D)}$$

Junction Capacitance



$$C_j = \frac{C_{j0}}{(1 - V_D / \phi_0)^m}$$

$m = 0.5$: abrupt junction
 $m = 0.33$: linear junction

$$C_{j0} = A_D \sqrt{\left[\frac{\epsilon_{si} q}{2} \frac{N_A N_D}{N_A + N_D} \right] \Phi_0^{-1}}$$

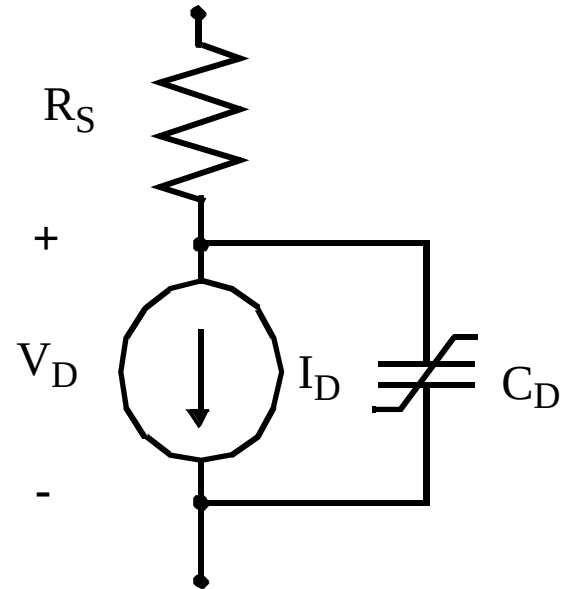
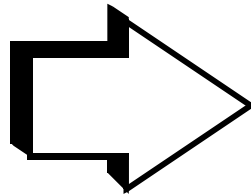
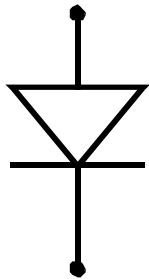
Large-Signal Depletion Region Capacitance

Junction capacitance is a voltage-dependent parameter. In digital circuits, operating voltages tend to move rapidly over a wide range $V_{\text{high}} - V_{\text{low}}$. It is more appropriate to replace the voltage dependent nonlinear capacitance C_j by an equivalent linear capacitance C_{eq}

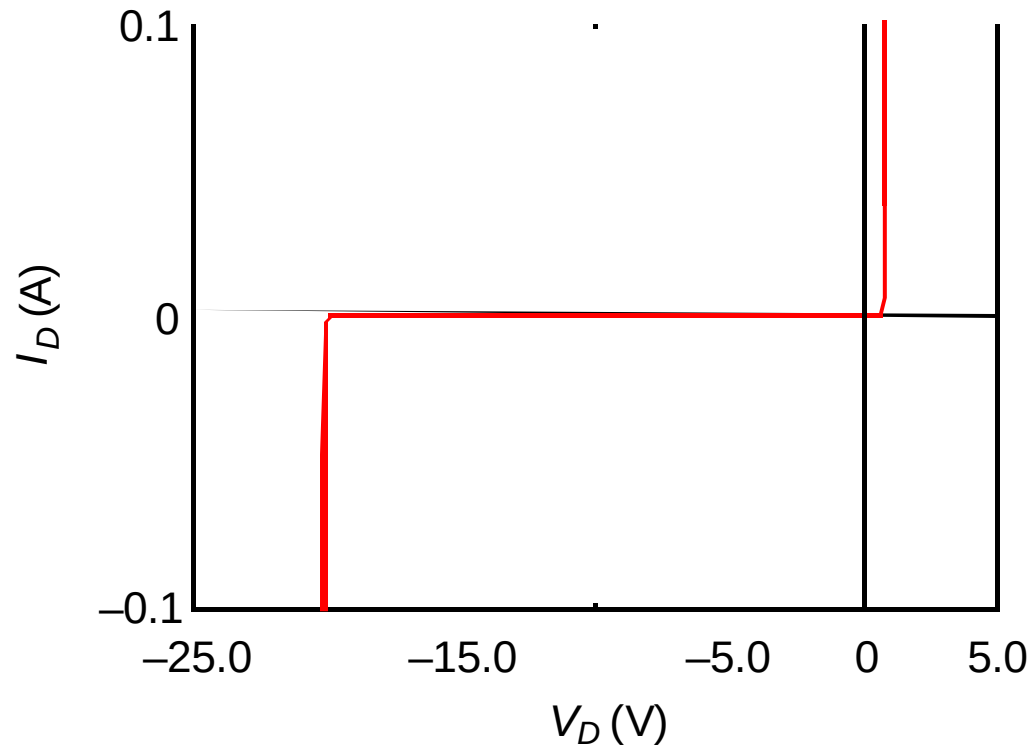
$$C_{\text{eq}} = \frac{\Delta Q_j}{\Delta V_D} = \frac{Q_j(\text{high}) - Q_j(\text{low})}{V_{\text{high}} - V_{\text{low}}} = K_{\text{eq}} C_{j0}$$

$$K_{\text{eq}} = \frac{-\Phi_0^m}{(V_{\text{high}} - V_{\text{low}})(1-m)} \left[(\Phi_0 - V_{\text{high}})^{1-m} - (\Phi_0 - V_{\text{low}})^{1-m} \right]$$

Diode Model



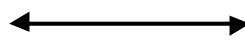
Secondary Effects



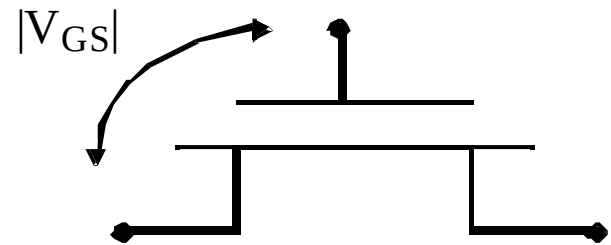
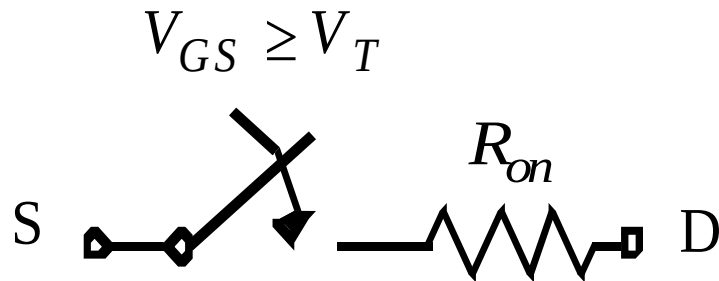
Avalanche Breakdown

What is a Transistor?

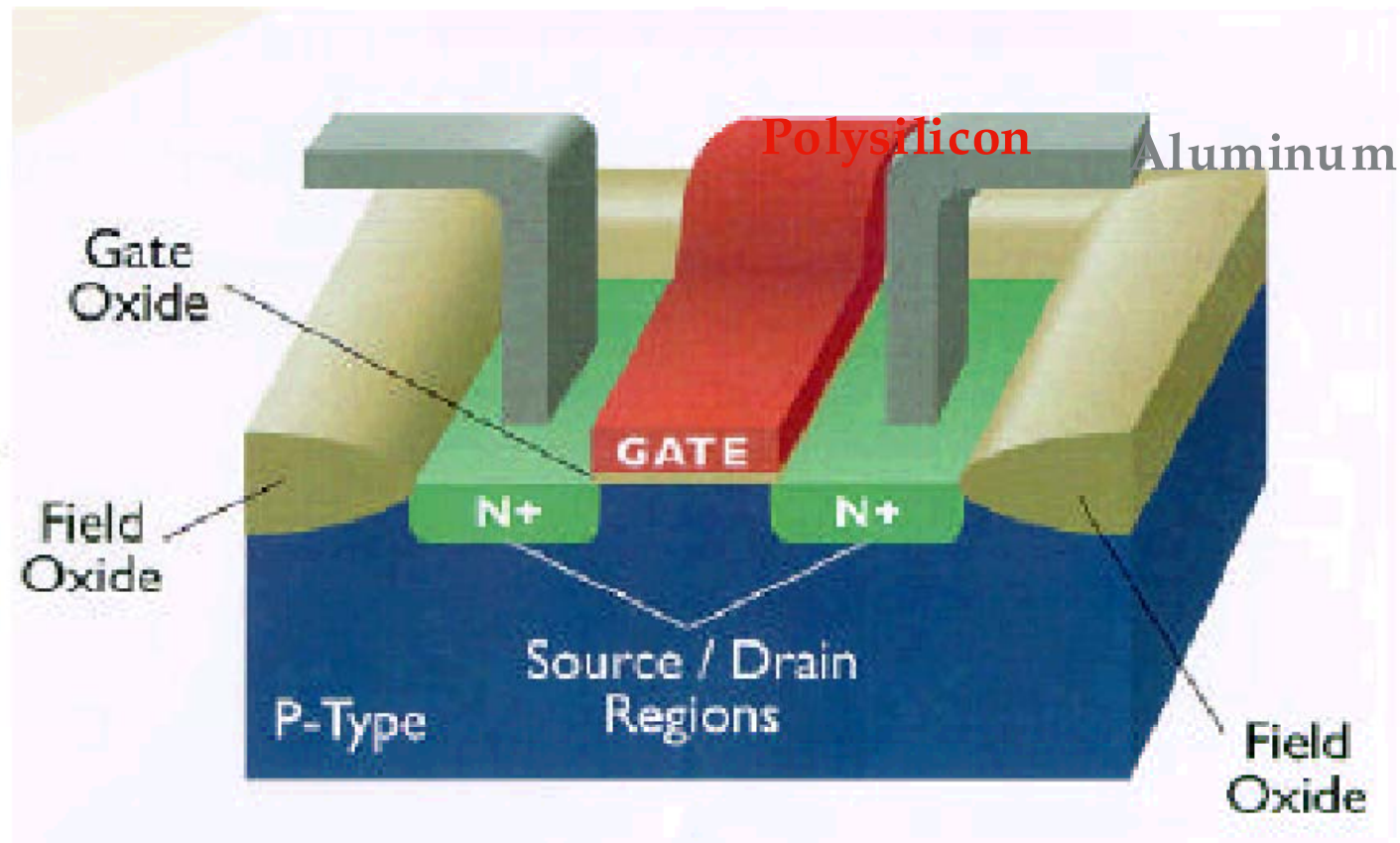
A Switch!

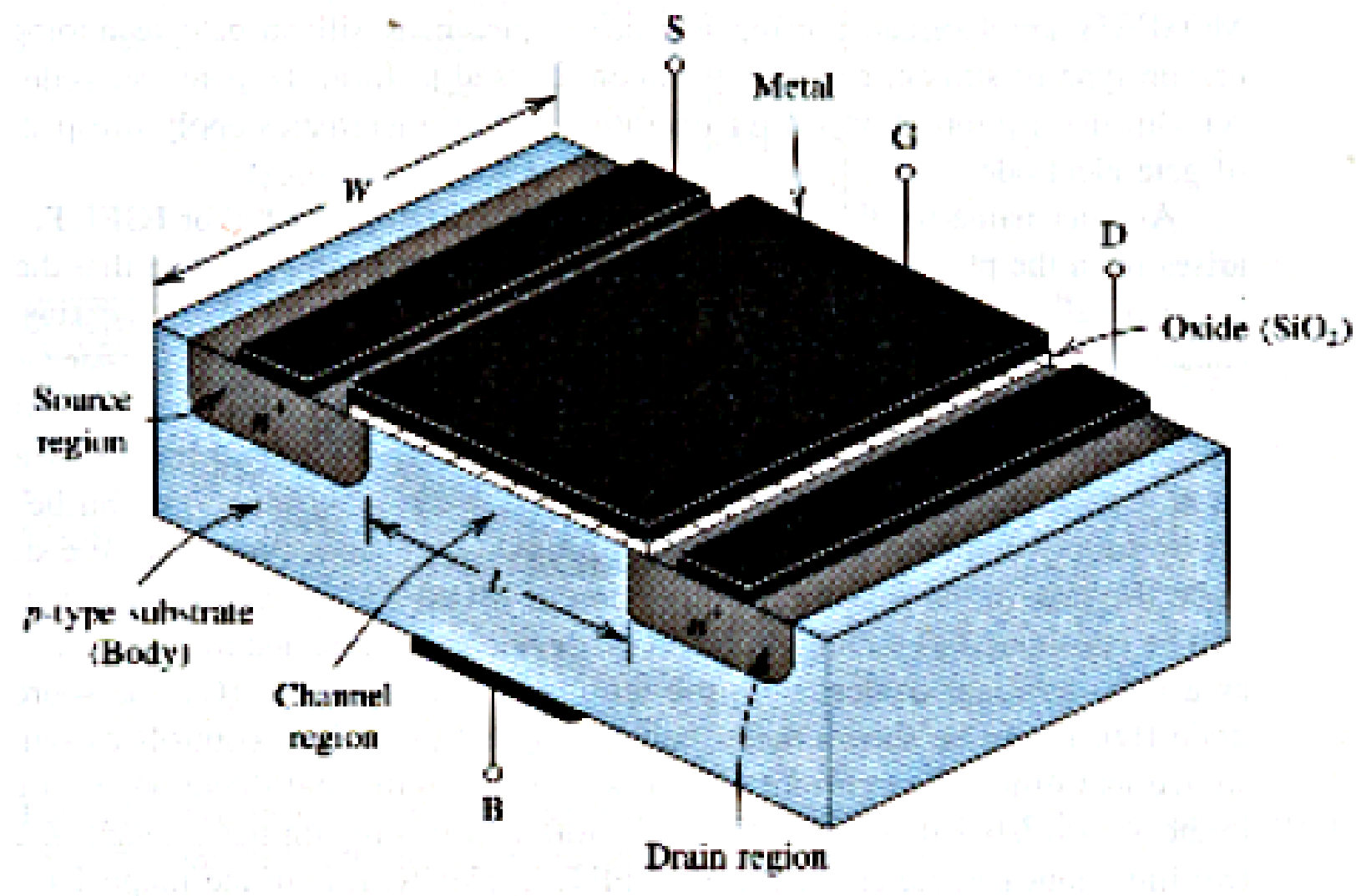


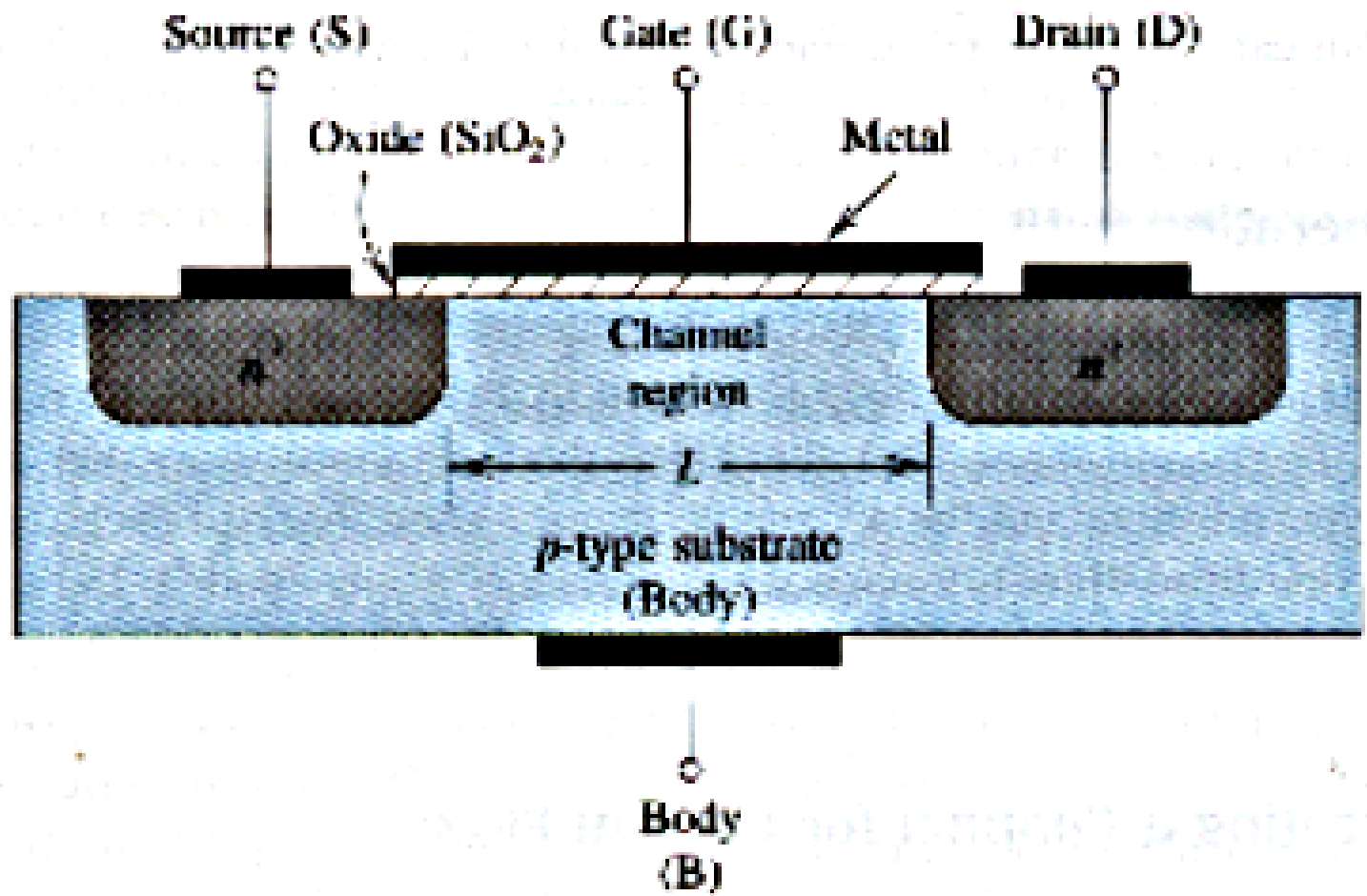
A MOS Transistor



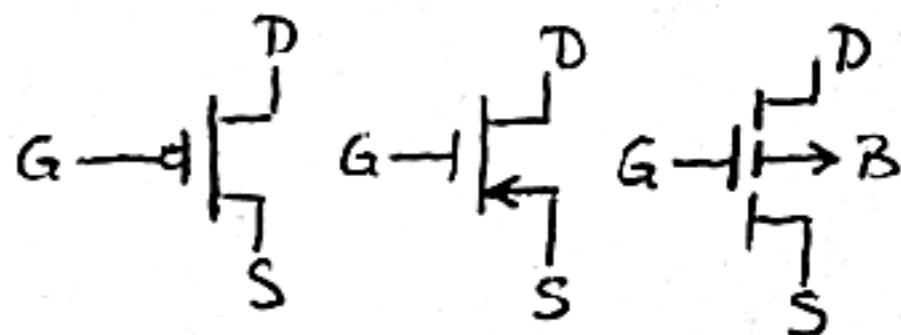
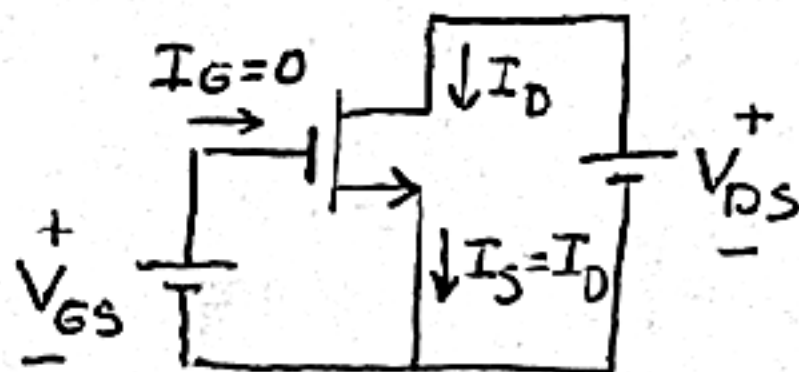
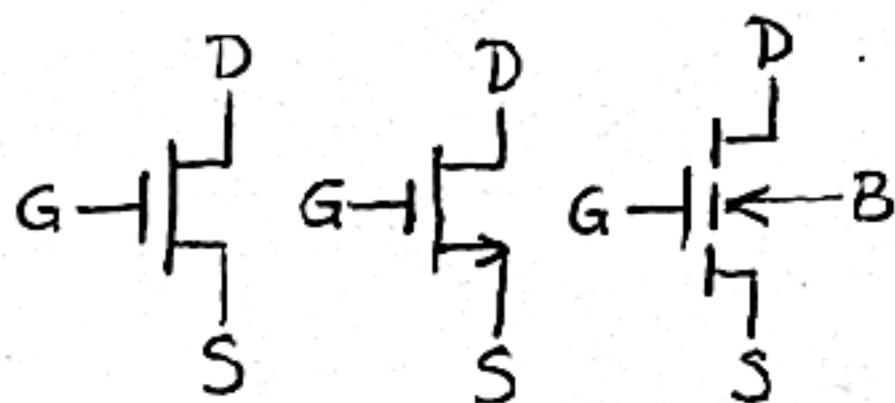
The MOS Transistor



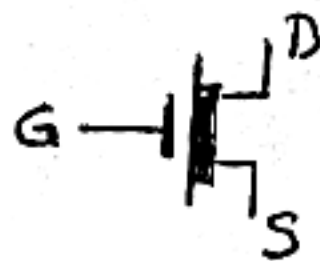
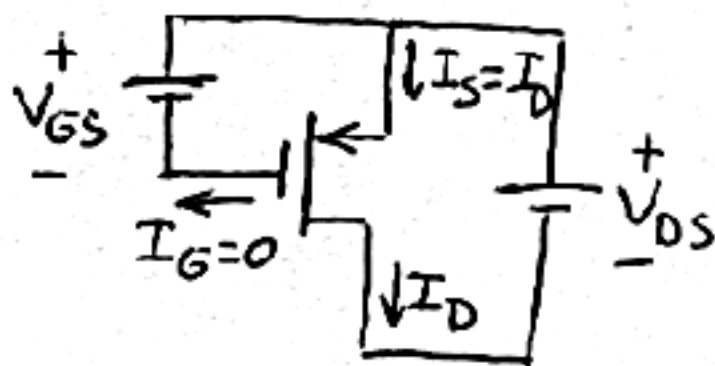




NMOS Enhancement

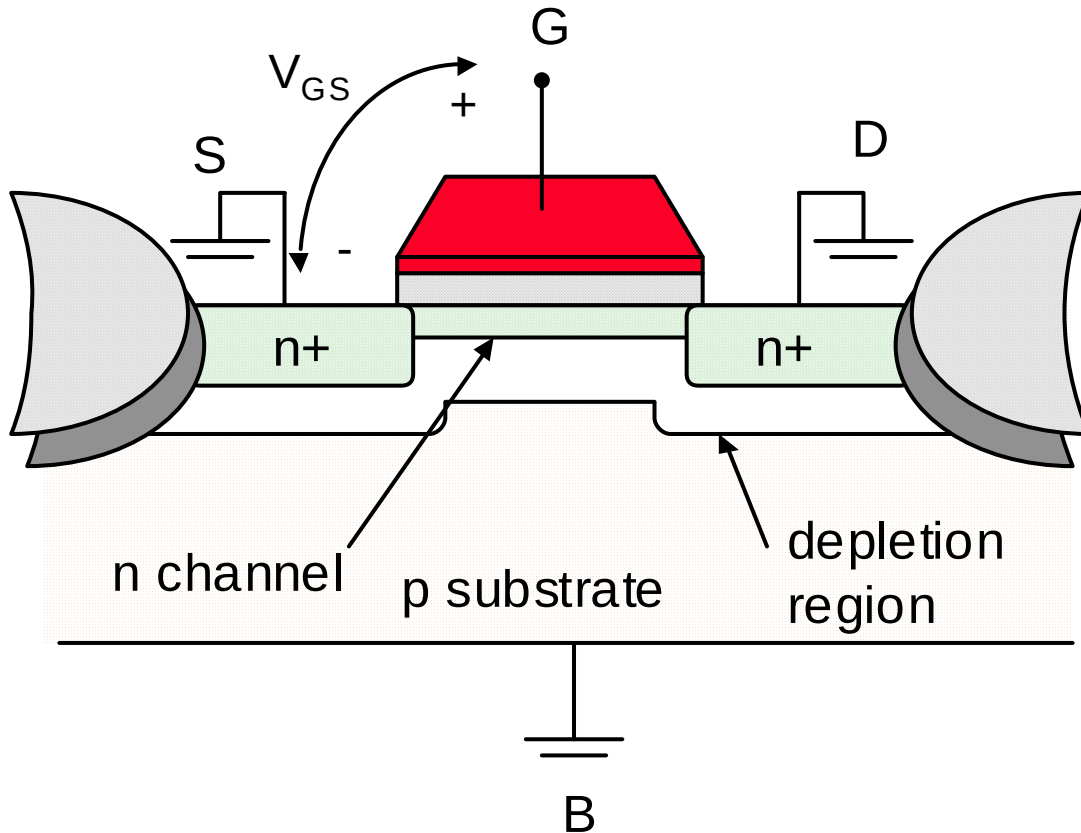


PMOS Enhancement



NMOS Depletion

Threshold Voltage Concept



The value of V_{GS} where strong inversion occurs is called the threshold voltage, V_T

$$W_d = \sqrt{\frac{2\epsilon_{si} \Phi}{q N_A}} \quad Q_d = \sqrt{2q N_A \epsilon_{si} \Phi}$$

Where ϕ is the voltage across the depletion layer (potential at the oxide-silicon boundary, N_A is the substrate doping.

In the presence of an inversion layer, the charge stored in the depletion region is fixed and equal to:

$$Q_{B0} = \sqrt{2q N_A \epsilon_{si} |2\Phi_F|}$$

When a substrate bias voltage V_{SB} is applied, the surface potential required for strong inversion increases and the charge stored can be expressed as:

$$Q_B = \sqrt{2q N_A \epsilon_{si} (|(-2)\Phi_F + V_{SB}|)}$$

The Threshold Voltage

where

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

V_{T0} is the threshold voltage at $V_{SB} = 0$ and is mostly a function of the manufacturing process

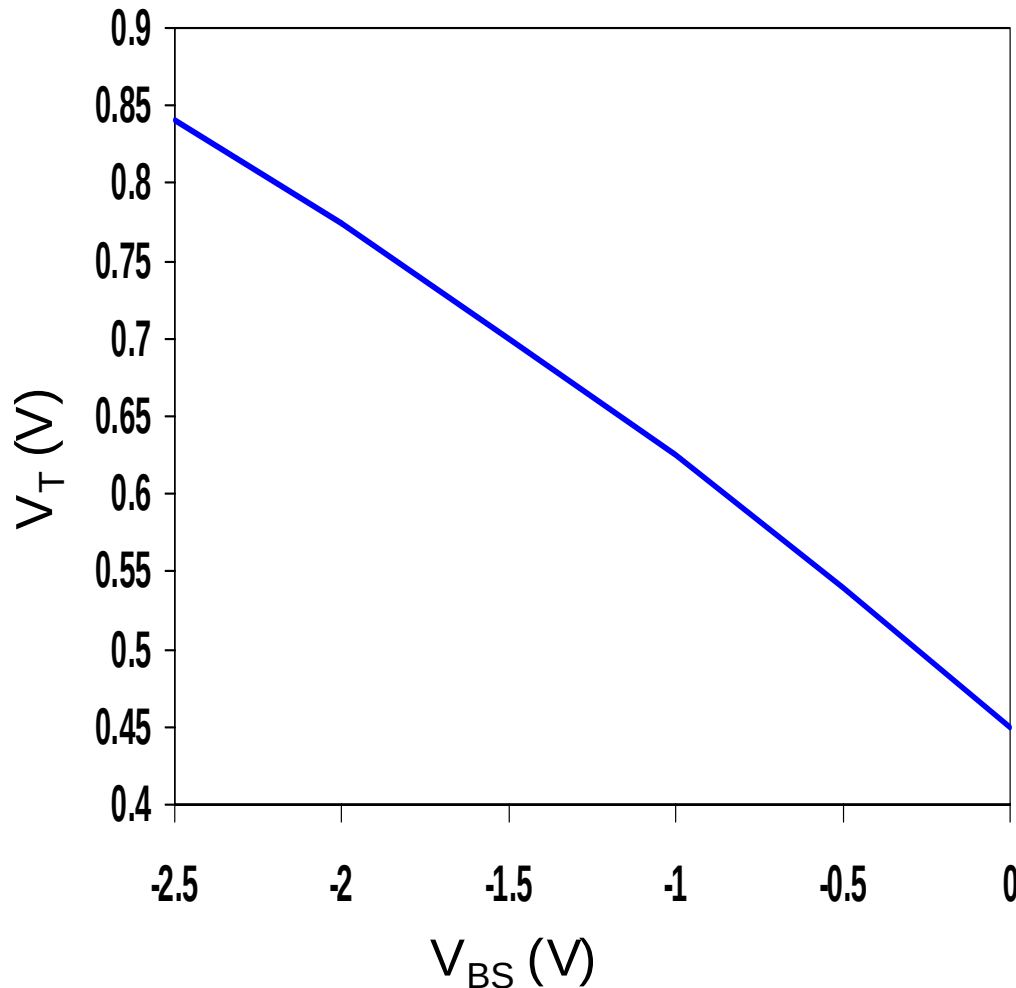
λ Difference in work-function between gate and substrate material, oxide thickness, Fermi voltage, charge of impurities trapped at the surface, dosage of implanted ions, etc.

V_{SB} is the source-bulk voltage

$\phi_F = -\phi_T \ln(N_A/n_i)$ is the **Fermi potential** ($\sim -0.3V$) ($\phi_T = kT/q = 26mV$ at 300K is the thermal voltage; N_A is the acceptor ion concentration; $n_i \approx 1.5 \times 10^{10} \text{ cm}^{-3}$ at 300K is the intrinsic carrier concentration in pure silicon)

$\gamma = \sqrt{(2q\epsilon_{Si}N_A)/C_{ox}}$ is the **body-effect coefficient** (impact of changes in V_{SB}) ($\epsilon_{Si} = 1.053 \times 10^{-10} \text{ F/m}$ is the permittivity of silicon; $C_{ox} = \epsilon_{ox}/t_{ox}$ is the gate oxide capacitance with $\epsilon_{ox} = 3.5 \times 10^{-11} \text{ F/m}$)

The Body Effect

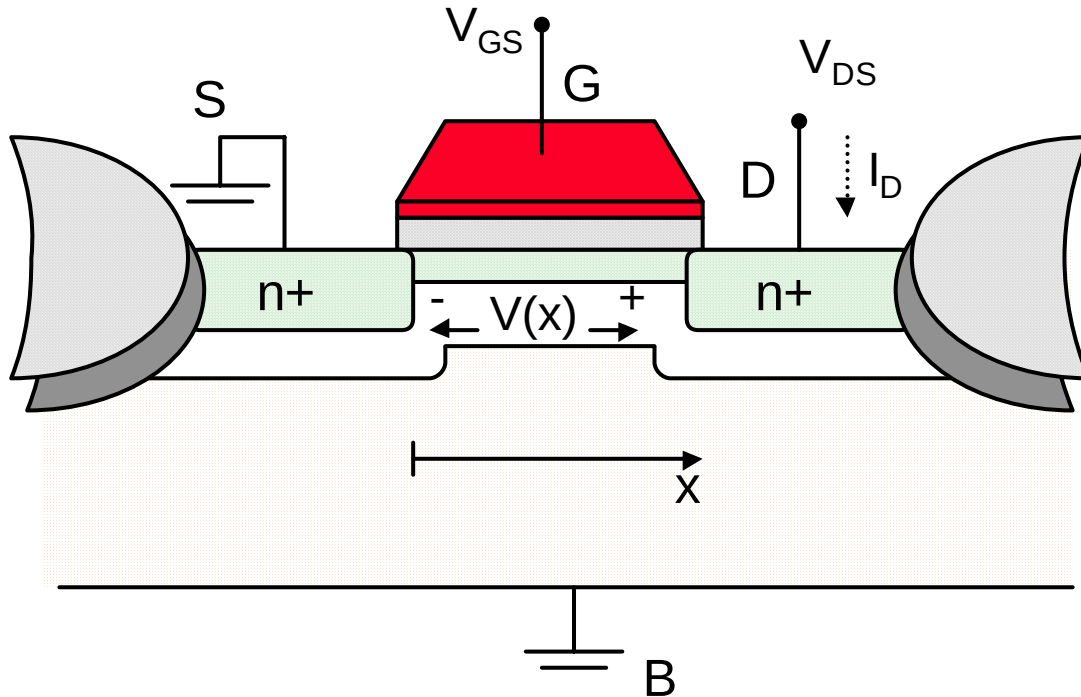


λ V_{SB} is the substrate bias voltage (normally positive for n-channel devices with the body tied to ground)

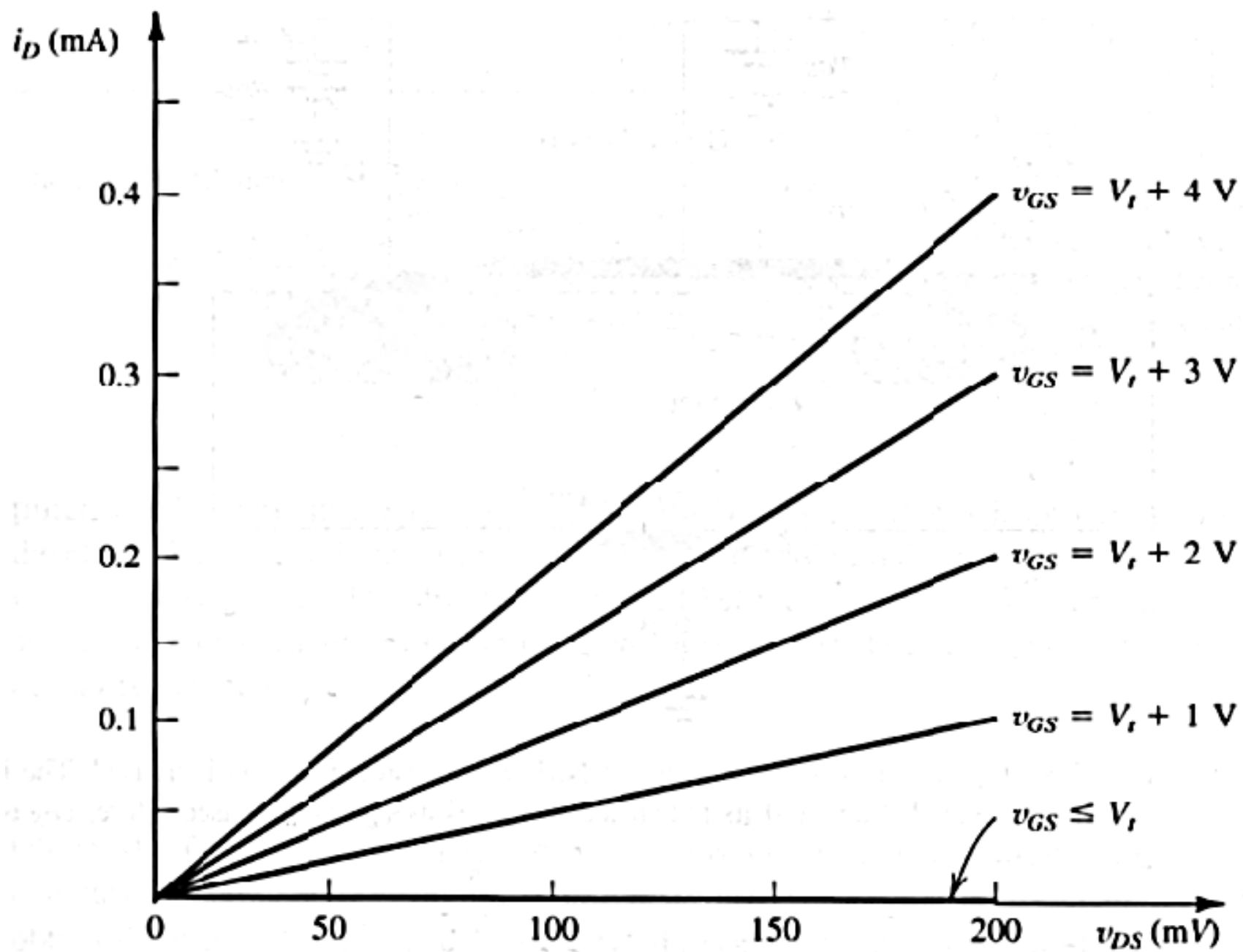
λ A negative bias causes V_T to increase from 0.45V to 0.85V

Transistor in Linear Mode

Assuming $V_{GS} > V_T$

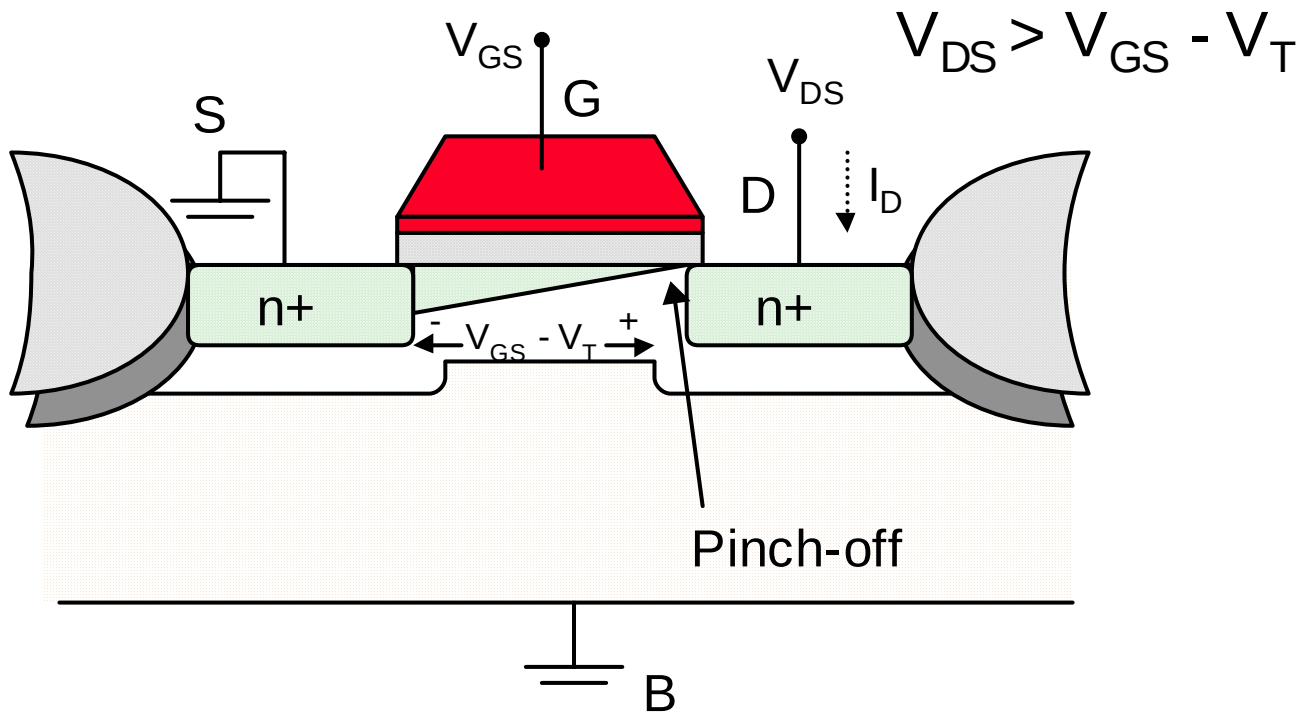


The current is a linear function of both V_{GS} and V_{DS}

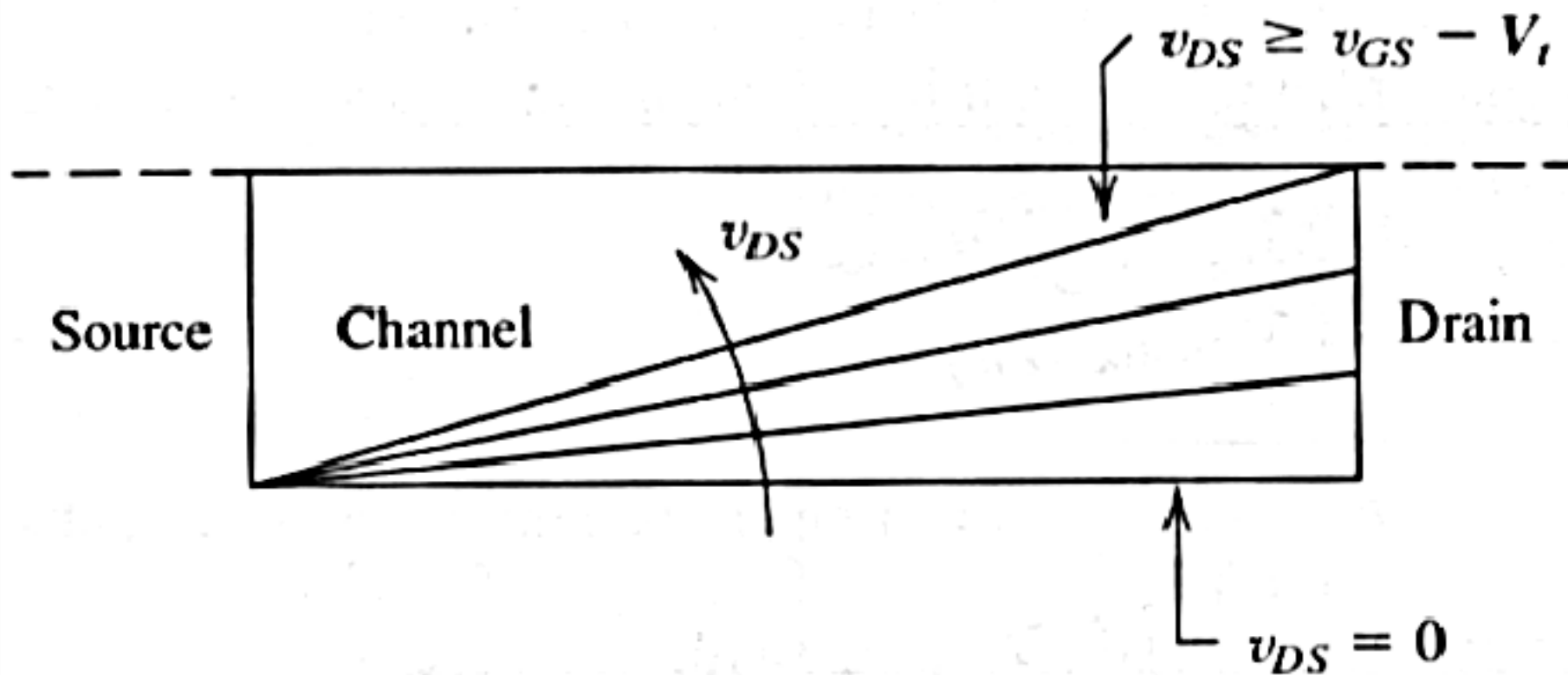


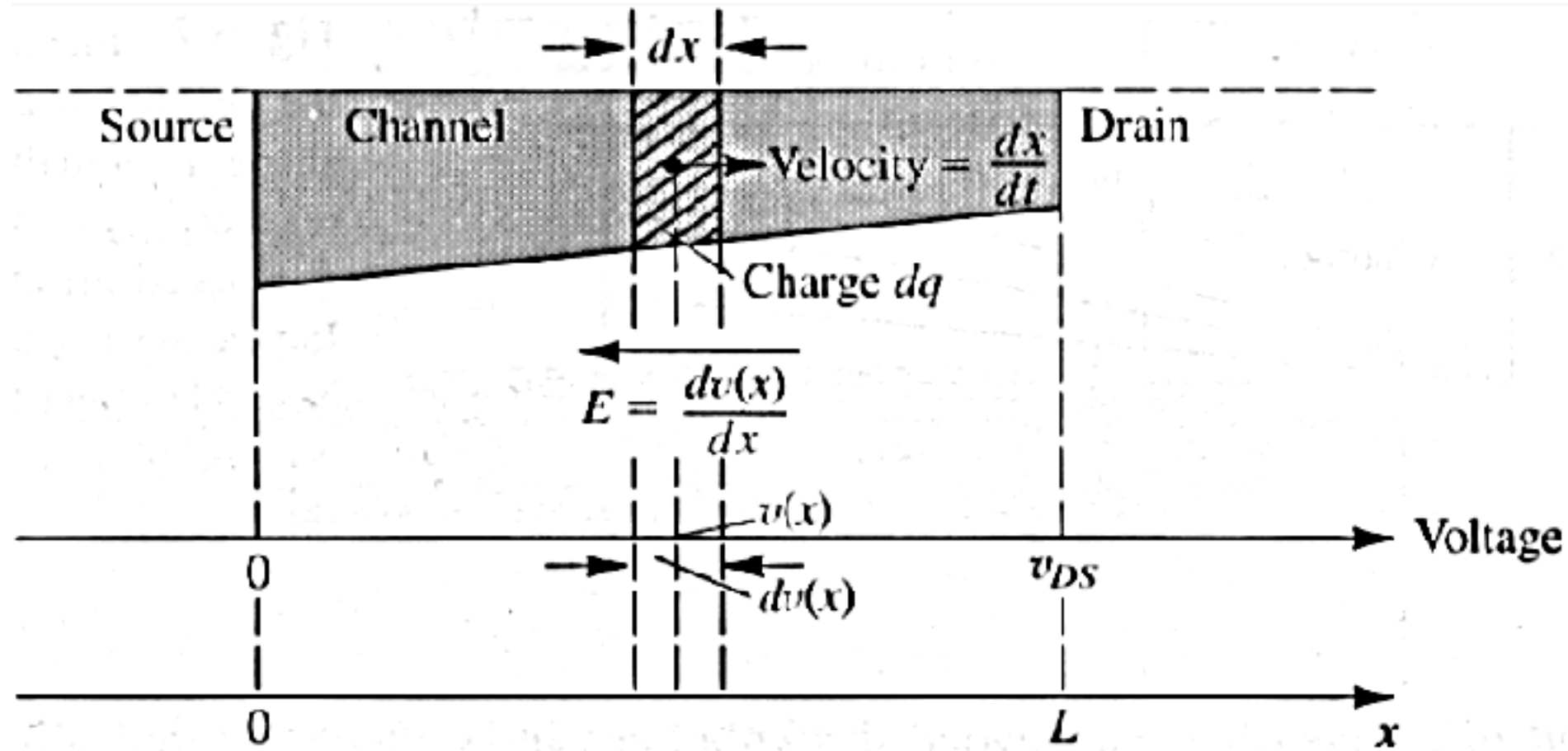
Transistor in Saturation Mode

Assuming $V_{GS} > V_T$



The current remains constant (saturates).





Assuming $V_{GS} > V_T$ and $V_{DS} < V_{GS} - V_T$ (resistive operation)

Resistive Operation:

$$dq(x) = -C_{ox} W dx [V_{GS} - v(x) - V_T] \dots\dots\dots (1)$$

where $dq(x)$ is the charge in an infinitesimal portion of the channel.

$$\text{Charge per unit area: } Q_i(x) = \frac{dq(x)}{dxW} = -C_{ox} [V_{GS} - v(x) - V_T]$$

$$\text{Capacitance per unit area: } C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \text{ where, } \epsilon_{ox} : \text{oxide permittivity,}$$

$$t_{ox} : \text{oxide thickness. The electric field at point } x: E(x) = -\frac{dv(x)}{dx}$$

$E(x)$ causes the electron charge $dq(x)$ to drift toward the drain

$$\text{with a velocity } \frac{dx}{dt} = v_n = -\mu_n E(x) = \mu_n \frac{dv(x)}{dx}$$

$$\text{since, } i = \frac{dq}{dt} = \frac{dx}{dt} \frac{dq(x)}{dx} = \mu_n \frac{dv(x)}{dx} \frac{dq(x)}{dx} \dots\dots\dots (2)$$

Using (1) $\rightarrow \frac{dq(x)}{dx} = -C_{ox} W [V_{GS} - v(x) - V_T]$

inserting into (2) $\rightarrow i = -\mu_n C_{ox} W [V_{GS} - v(x) - V_T] \frac{dv(x)}{dx}$

$I_D = -i = \mu_n C_{ox} W [V_{GS} - v(x) - V_T] \frac{dv(x)}{dx}$ rearranging & integrating both

sides: $\int_0^L I_D dx = \int_0^{V_{DS}} \mu_n C_{ox} W [V_{GS} - V_T - v(x)] dv(x)$

$\swarrow$ $v(L)$
 $\nwarrow$ $v(0)$

$$I_D = (\mu_n C_{ox}) \left(\frac{W}{L} \right) \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

where: $\mu_n C_{ox} = K'_n$: process transconductance parameter,

$K_n = K'_n \frac{W}{L}$: gain factor, $\frac{W}{L}$: aspect ratio

