



Başkent Üniversitesi
Elektrik Elektronik Müh. Bölümü
EEM312 – DIGITAL ELECTRONIC
Laboratory

Report

02.06.2005

Experiment No : Y8

Experiment Name : Mantık Kapısı Tasarımı

[Redacted]

[Redacted]

[Redacted]

[Redacted]

Number

[Redacted]

[Redacted]

1-) XOR Kapısı

*laby8

```
.MODEL MOSN NMOS LEVEL=2 LD=0.15U TOX=200.0E-10
+ NSUB=5.36726E+15 VTO=0.743469 KP=8.00059E-05 GAMMA=0.543
+ PHI=0.6 U0=655.881 UEXP=0.157282 UCRIT=31443.8
+ DELTA=2.39824 VMAX=55260.9 XJ=0.25U LAMBDA=0.0367072
+ NFS=1E+12 NEFF=1.001 NSS=1E+11 TPG=1.0 RSH=70.00
+ CGDO=4.3E-10 CGSO=4.3E-10 CJ=0.0003 MJ=0.6585
+ CJSW=8.0E-10 MJSW=0.2402 PB=0.58
```

```
.MODEL MOSP PMOS LEVEL=2 LD=0.15U TOX=200.0E-10
+ NSUB=4.3318E+15 VTO=-0.738861 KP=2.70E-05 GAMMA=0.58
+ PHI=0.6 U0=261.977 UEXP=0.323932 UCRIT=65719.8
+ DELTA=1.79192 VMAX=25694 XJ=0.25U LAMBDA=0.0612279
+ NFS=1E+12 NEFF=1.001 NSS=1E+11 TPG=-1.0 RSH=120.6
+ CGDO=4.3E-10 CGSO=4.3E-10 CJ=0.0005 MJ=0.5052
+ CJSW=1.349E-10 MJSW=0.2417 PB=0.64
```

M1 5 1 4 4 MOSP W=5.4u L=1.2u

M2 3 2 1 4 MOSP W=5.4u L=1.2u

M3 3 1 2 4 MOSP W=5.4u L=1.2u

M4 5 1 0 0 MOSN W=1.8u L=1.2u

M5 2 5 3 0 MOSN W=1.8u L=1.2u

M6 3 2 5 0 MOSN W=1.8u L=1.2u

vdd 4 0 5V

Vin 1 0 pulse(0V 5V 0 0ns 0ns 100ns 200ns)

Vin1 2 0 pulse(0V 5V 0 0ns 0ns 200ns 400ns)

.control

tran 0.05n 400n

plot v(3)

plot v(1)

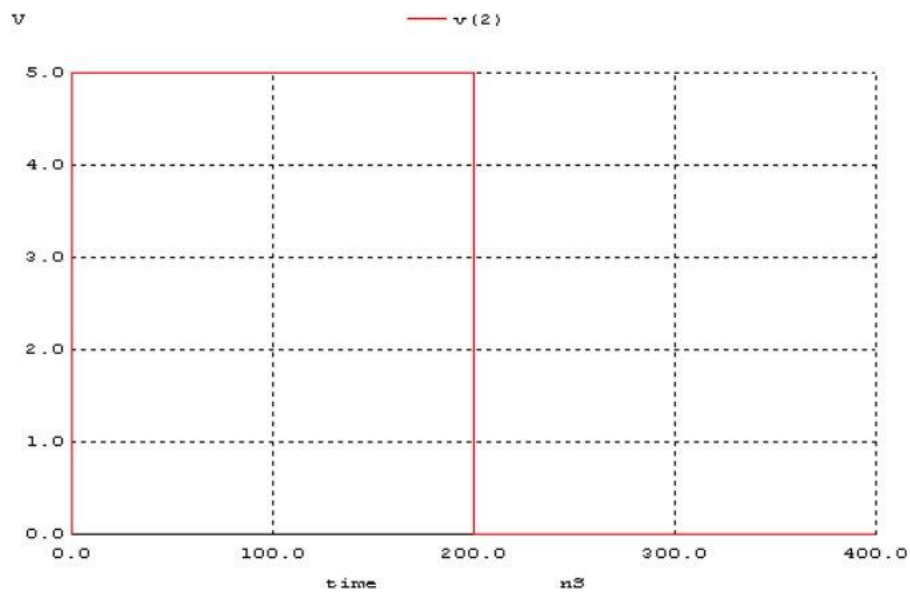
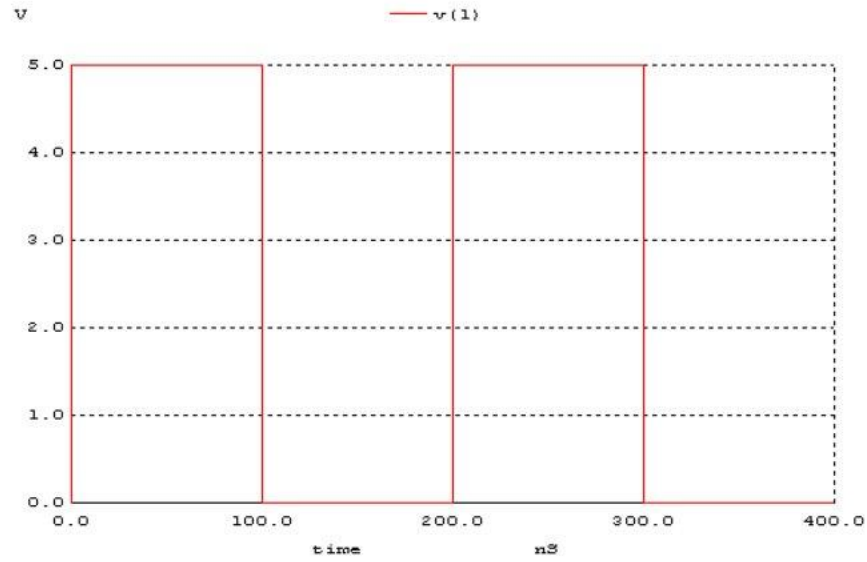
plot v(2)

.endc

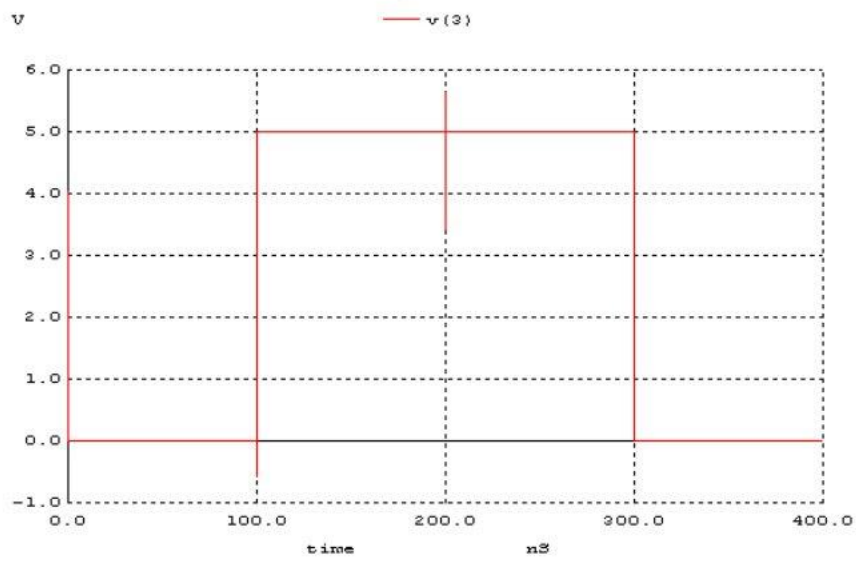
.end

V(1)	V(2)	XOR (v(3))
0	0	0
0	1	1
1	0	1
1	1	0

	Gecikme Süresi
Low to High	0,27 ns
High to Low	0,268 ns



(XOR Kapısının Girişleri)



(XOR Kapısının Çıkışı)

2-) NAND GATE

*laby8

```
.MODEL MOSN NMOS LEVEL=2 LD=0.15U TOX=200.0E-10
+ NSUB=5.36726E+15 VTO=0.743469 KP=8.00059E-05 GAMMA=0.543
+ PHI=0.6 U0=655.881 UEXP=0.157282 UCRIT=31443.8
+ DELTA=2.39824 VMAX=55260.9 XJ=0.25U LAMBDA=0.0367072
+ NFS=1E+12 NEFF=1.001 NSS=1E+11 TPG=1.0 RSH=70.00
+ CGDO=4.3E-10 CGSO=4.3E-10 CJ=0.0003 MJ=0.6585
+ CJSW=8.0E-10 MJSW=0.2402 PB=0.58
```

```
.MODEL MOSP PMOS LEVEL=2 LD=0.15U TOX=200.0E-10
+ NSUB=4.3318E+15 VTO=-0.738861 KP=2.70E-05 GAMMA=0.58
+ PHI=0.6 U0=261.977 UEXP=0.323932 UCRIT=65719.8
+ DELTA=1.79192 VMAX=25694 XJ=0.25U LAMBDA=0.0612279
+ NFS=1E+12 NEFF=1.001 NSS=1E+11 TPG=-1.0 RSH=120.6
+ CGDO=4.3E-10 CGSO=4.3E-10 CJ=0.0005 MJ=0.5052
+ CJSW=1.349E-10 MJSW=0.2417 PB=0.64
```

M1 5 2 1 1 MOSP W=5.4u L=1.2u

M2 5 3 1 1 MOSP W=5.4u L=1.2u

M3 5 4 1 1 MOSP W=5.4u L=1.2u

M4 5 2 7 7 MOSN W=1.8u L=1.2u

M5 7 3 9 9 MOSN W=1.8u L=1.2u

M6 9 4 0 0 MOSN W=1.8u L=1.2u

vdd 1 0 5V

Vin 2 0 pulse(5V 0V 0 1ns 1ns 100ns 200ns)

Vin1 3 0 pulse(5V 0V 0 1ns 1ns 200ns 400ns)

Vin2 4 0 pulse(5V 0V 0 1ns 1ns 400ns 800ns)

c1 5 0 1fF

.control

tran 0.05n 1600n

plot v(2)

plot v(3)

plot v(4)

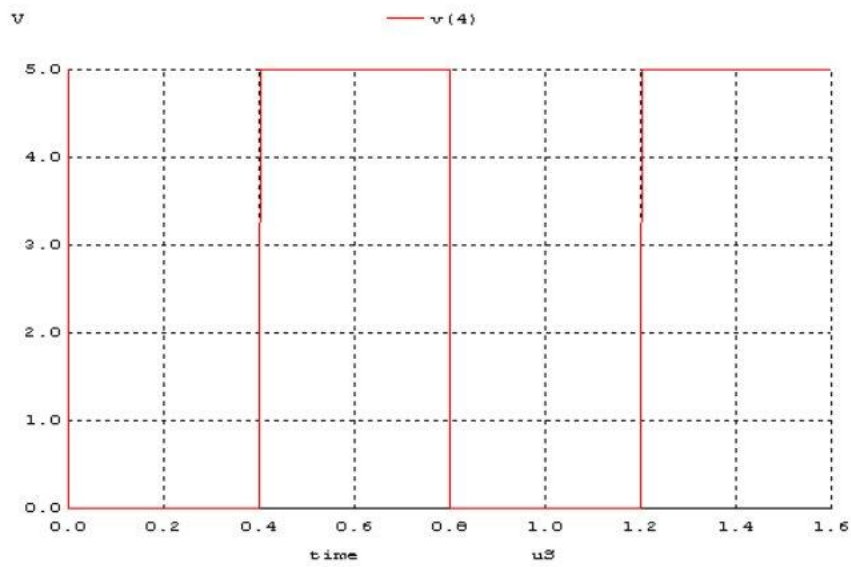
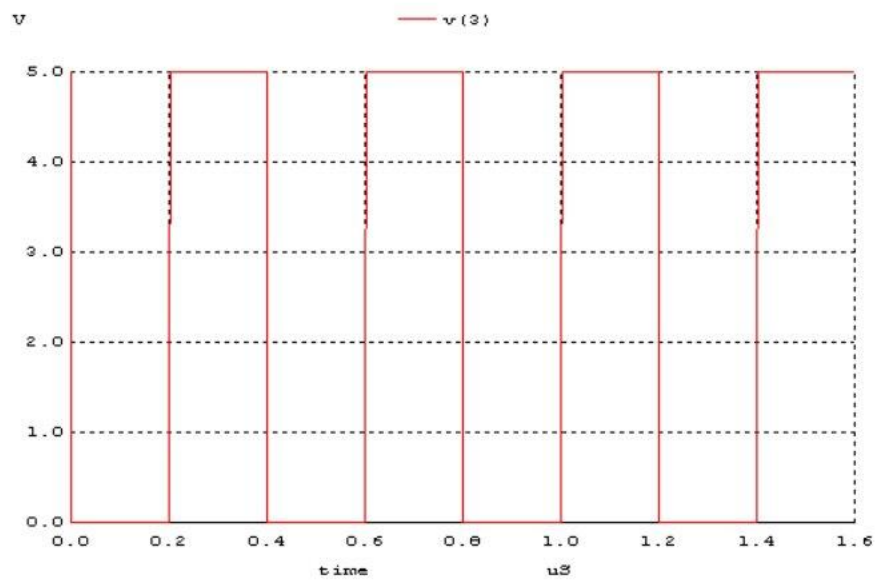
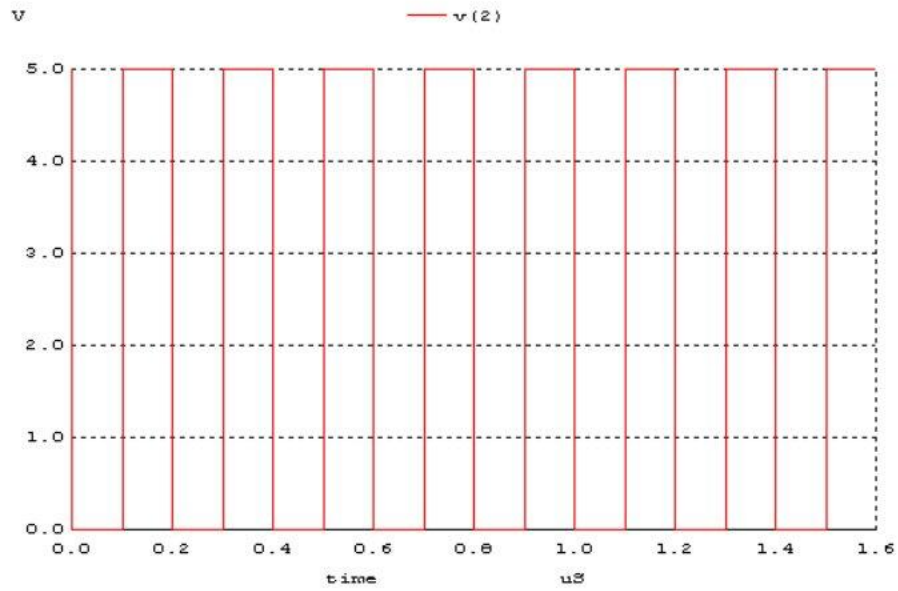
plot v(5)

.endc

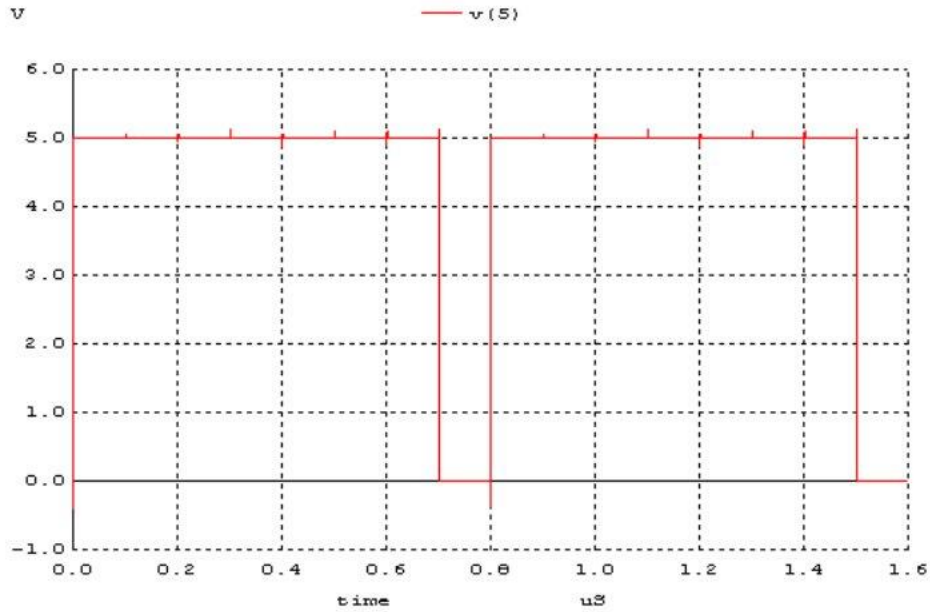
.end

V(2)	V(3)	V(4)	NAND (v(5))
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

	Gecikme Süresi
Low to High	1,03 ns
High to Low	2,35 ns



(NAND Kapısının Girişleri)



(NAND Kapısının Çıkışı)

3-) NOR GATE

*laby8

```
.MODEL MOSN NMOS LEVEL=2 LD=0.15U TOX=200.0E-10
+ NSUB=5.36726E+15 VTO=0.743469 KP=8.00059E-05 GAMMA=0.543
+ PHI=0.6 U0=655.881 UEXP=0.157282 UCRIT=31443.8
+ DELTA=2.39824 VMAX=55260.9 XJ=0.25U LAMBDA=0.0367072
+ NFS=1E+12 NEFF=1.001 NSS=1E+11 TPG=1.0 RSH=70.00
+ CGDO=4.3E-10 CGSO=4.3E-10 CJ=0.0003 MJ=0.6585
+ CJSW=8.0E-10 MJSW=0.2402 PB=0.58
```

```
.MODEL MOSP PMOS LEVEL=2 LD=0.15U TOX=200.0E-10
+ NSUB=4.3318E+15 VTO=-0.738861 KP=2.70E-05 GAMMA=0.58
+ PHI=0.6 U0=261.977 UEXP=0.323932 UCRIT=65719.8
+ DELTA=1.79192 VMAX=25694 XJ=0.25U LAMBDA=0.0612279
+ NFS=1E+12 NEFF=1.001 NSS=1E+11 TPG=-1.0 RSH=120.6
+ CGDO=4.3E-10 CGSO=4.3E-10 CJ=0.0005 MJ=0.5052
+ CJSW=1.349E-10 MJSW=0.2417 PB=0.64
```

M1 7 2 0 0 MOSN W=1.8u L=1.2u

M2 7 4 0 0 MOSN W=1.8u L=1.2u

M3 7 6 0 0 MOSN W=1.8u L=1.2u

M4 3 2 1 1 MOSP W=5.4u L=1.2u

M5 5 4 3 3 MOSP W=5.4u L=1.2u

M6 7 6 5 5 MOSP W=5.4u L=1.2u

vdd 1 0 5V

Vin 2 0 pulse(5V 0V 0 1ns 1ns 100ns 200ns)

Vin1 4 0 pulse(5v 0V 0 1ns 1ns 200ns 400ns)

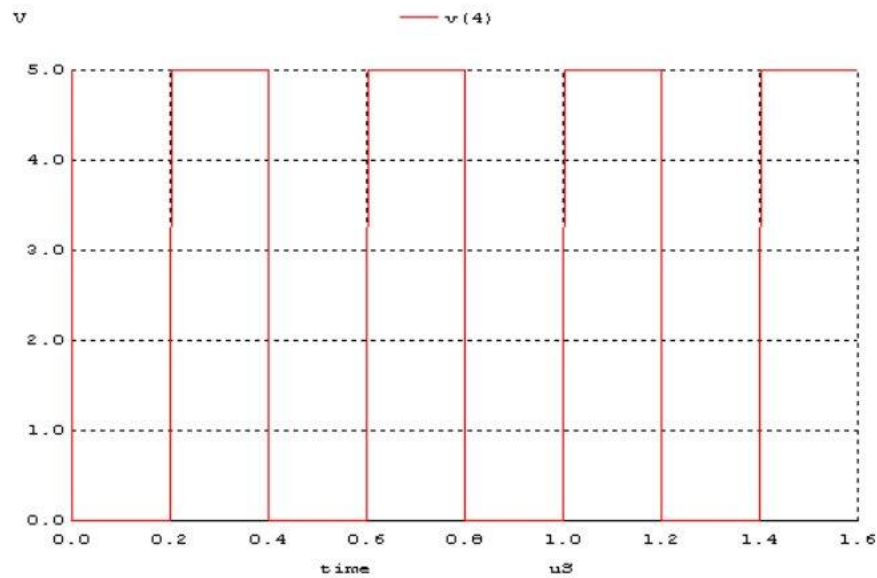
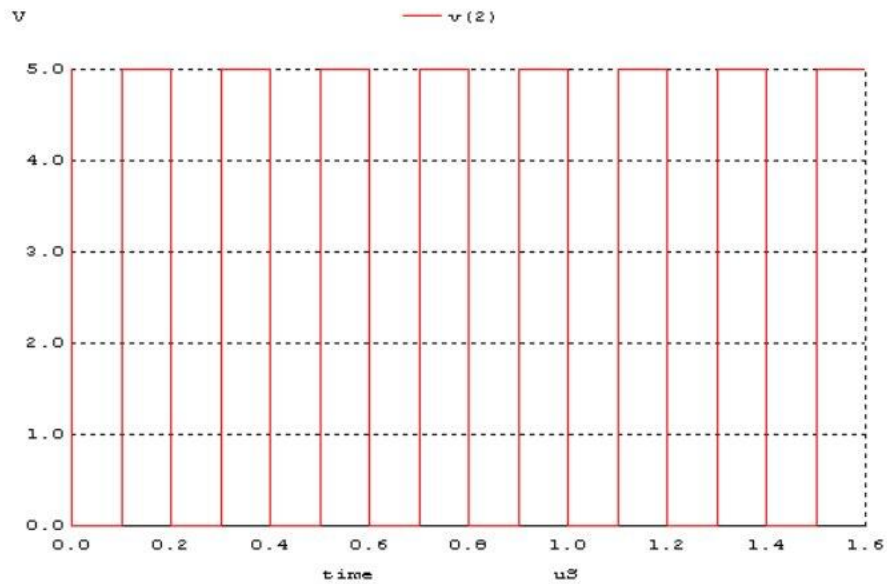
Vin2 6 0 pulse(5V 0V 0 1ns 1ns 400ns 800ns)

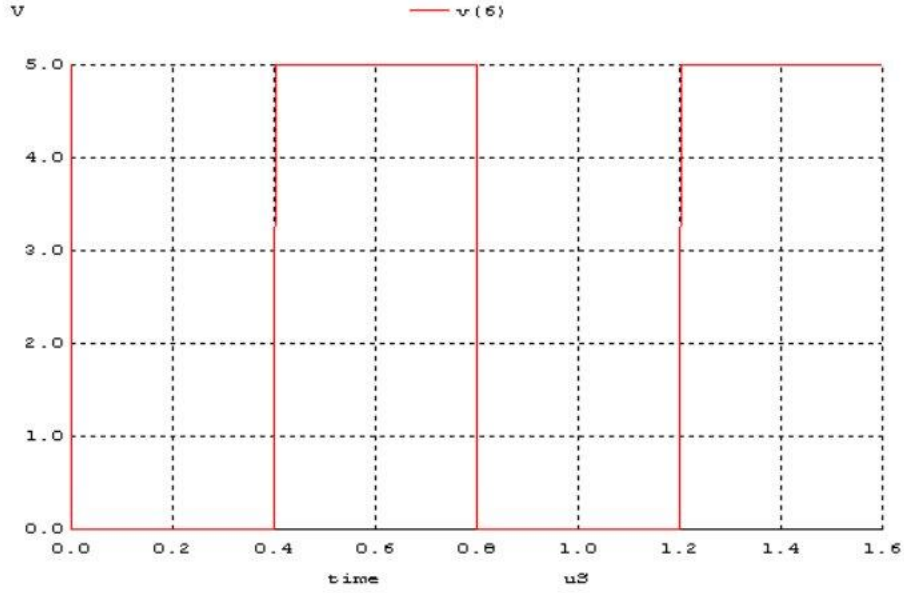
c1 7 0 1fF

```
.control  
tran 0.05n 1600n  
plot v(2)  
plot v(4)  
plot v(6)  
plot v(7)  
.endc  
.end
```

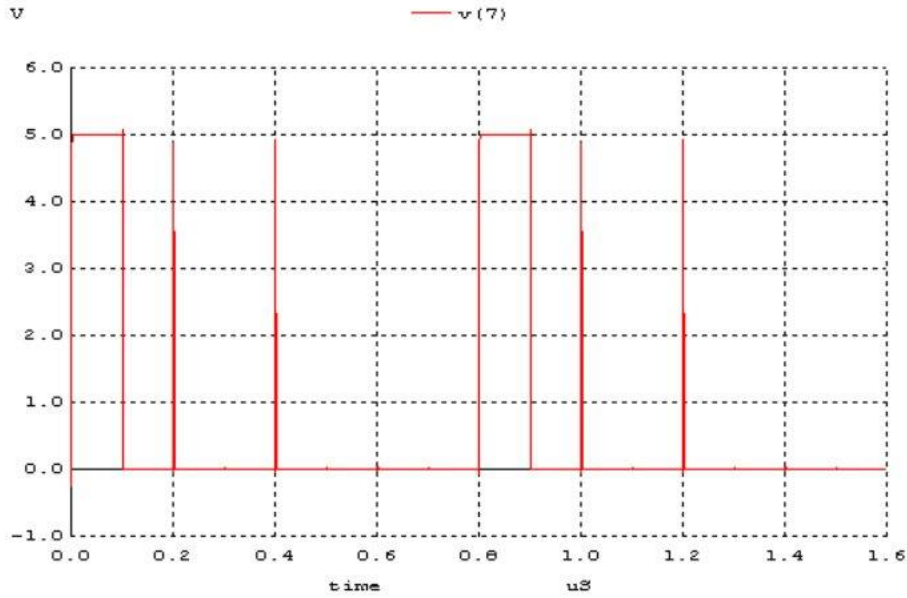
V(2)	V(4)	V(6)	NAND (v(7))
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

	Gecikme Süresi
Low to High	1,95 ns
High to Low	3,15 ns





(NOR Kapısı Girişleri)



(NOR Kapısı Çıkışı)

Üç kapı karşılaştırıldığında en az gecikme XOR kapısında çıkmıştır. Fakat XOR kapısı 2 girişli diğer iki kapı 3 girişlidir. Bu nedenle NOR ve NAND kapısını karşılaştırmak daha mantıklı olacaktır. NAND ve NOR kapısı karşılaştırıldığında NOR kapısında gecikme daha fazla çıkmıştır. Bunun nedeni NOR kapısının yapısı incelendiğinde transistörler paralel bağlanmıştır. NAND kapısında ise transistörler seri bağlanmıştır. NOR kapısında transistörler paralel bağlandığından gecikme fazla olmaktadır.