

8086 Hardware design

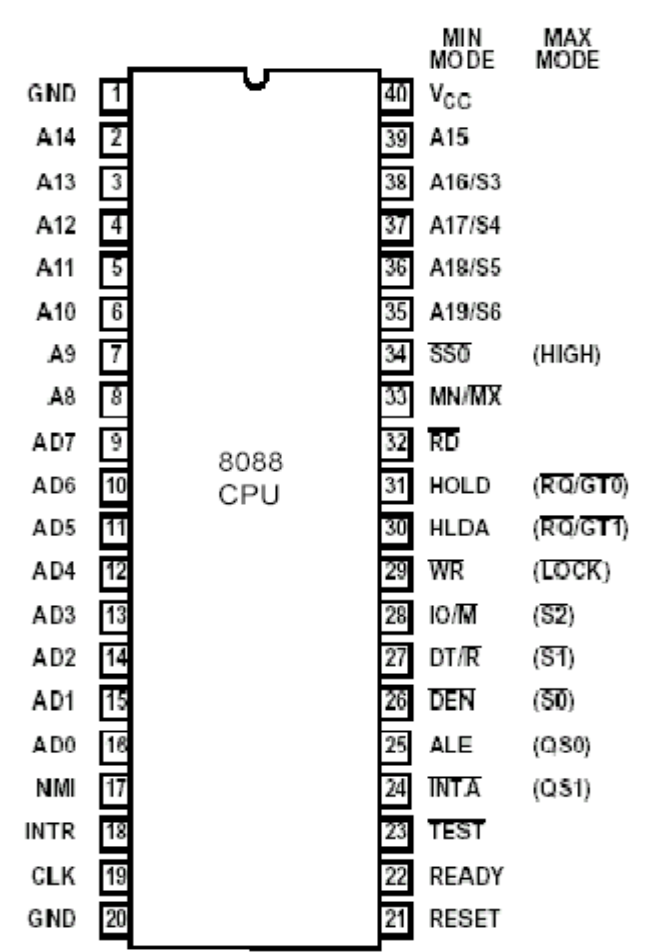
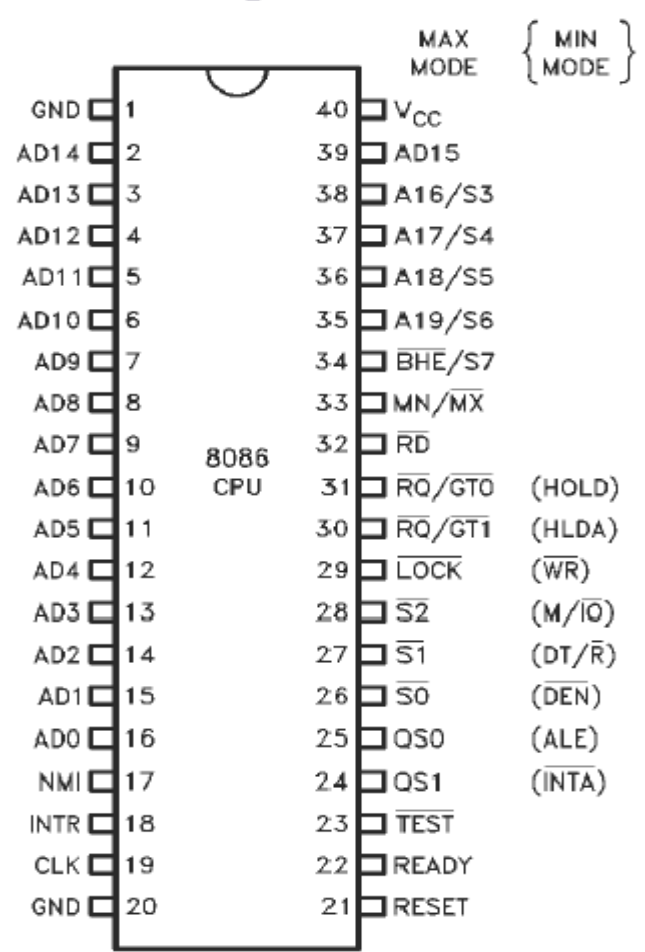
The 8086 and 8088 microprocessors can be configured to work in either of two modes:

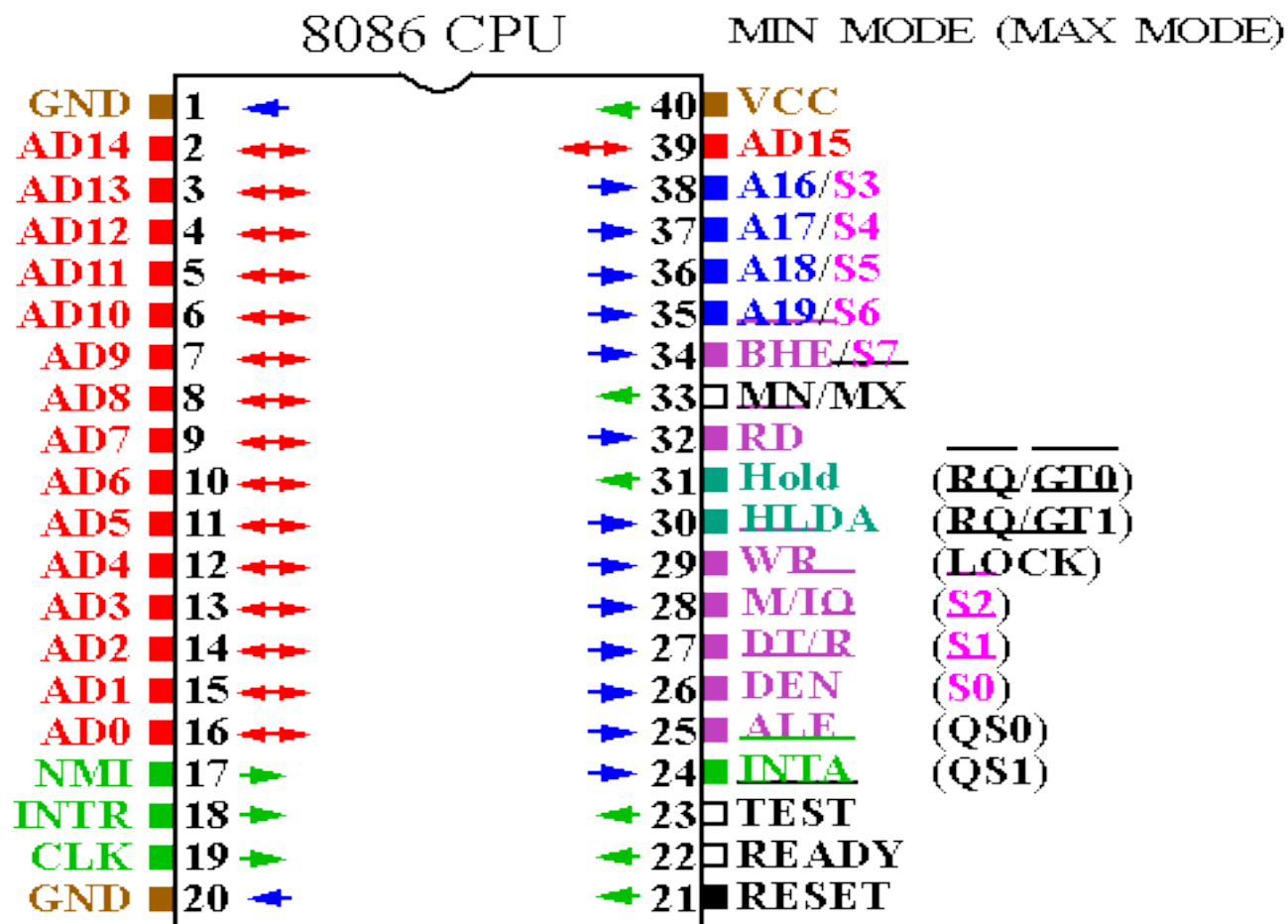
The minimum mode -

The maximum mode -

The mode selection feature lets the 8088 or 8086 better meet the needs of a wide variety of system requirement. Minimum mode 8088/8086 systems are typically smaller and contain a single processor.

Depending on the mode of operation selected, the assignment for a number of the pins on the microprocessor package are changed.





The minimum-mode signals can be divided into the following basic groups:

- ❖ Address/Data bus
- ❖ Status signals
- ❖ Control signals
- ❖ Interrupt signals
- ❖ DMA interface signals

Minimum-Mode Interface

Address/Data bus

The address bus is used to carry address information to the memory and I/O ports. The address bus is 20-bit long and consists of signal lines A0 through A19. A 20-bit address gives the 8088 a 1 Mbyte memory address space. Only address line A0 through A15 are used when addressing I/O. This give an I/O address space 64 Kbytes. The 8088 has 8 multiplexed address/data bus lines (A0~A7) while 8086 has 16 multiplexed address/data bus lines (A0~A15).

Control signals:

The **control signals** are provided to support the memory and I/O interfaces of the 8088 and 8086.

- ALE – Address Latch Enable
- $\text{IO}/\overline{\text{M}}$ – IO/Memory (8088)
- $\text{M}/\overline{\text{IO}}$ – Memory/IO (8086)
- $\text{DT}/\overline{\text{R}}$ – Data Transmit/Receive (8088/8086)
- $\overline{\text{SSO}}$ – System Status Output (8088)
- $\overline{\text{BHE}}$ – Bank High Enable (8086)
- $\overline{\text{RD}}$ – Read (8088/8086)
- $\overline{\text{WR}}$ – Write (8088/8086)
- $\overline{\text{DEN}}$ – Data Enable (8088/8086)
- READY – Ready (8088/8086)

RESET : Microprocessor resets if this pin is held high for 4 clock periods.

Interrupt signals

❖ The ***interrupt signals*** can be used by an external device to signal that it needs to be serviced.

- INTR – Interrupt Request
- INTA – Interrupt Acknowledge
- TEST – Test (can be use to synchronize MPU)
- NMI – Nonmaskable Interrupt
- RESET – Reset (hardware reset of the MPU)

8.6 System Clock

The time base for synchronization of the internal and external operations of the microprocessor in a microcomputer system is provided by the ***clock*** (CLK) input signal.

The standard 8088 operates at 5 MHz and the 8088- 2 operates at 8 MHz.

The 8086 is manufactured in three speeds: 5-MHz 8086, 8-MHz 8086-2, and the 10-MHz 8086-1.

The CLK is externally generated by the 8284 clock generator and driver IC.

System Clock

The time base for synchronization of the internal and external operations of the microprocessor in a microcomputer system is provided by the **clock** (CLK) input signal.

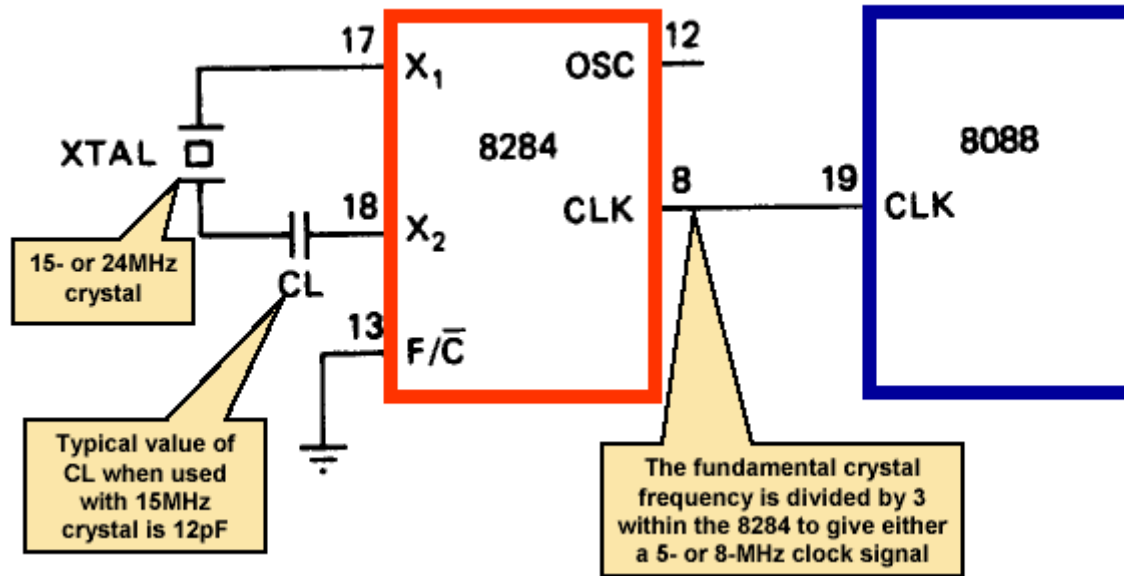
The standard 8088 operates at 5 MHz and the 8088-2 operates at 8 MHz.

The 8086 is manufactured in three speeds: 5-MHz 8086, 8-MHz 8086-2, and the 10-MHz 8086-1.

The CLK is externally generated by the 8284 clock generator and driver IC.

System Clock

Connecting the 8284 to the 8088



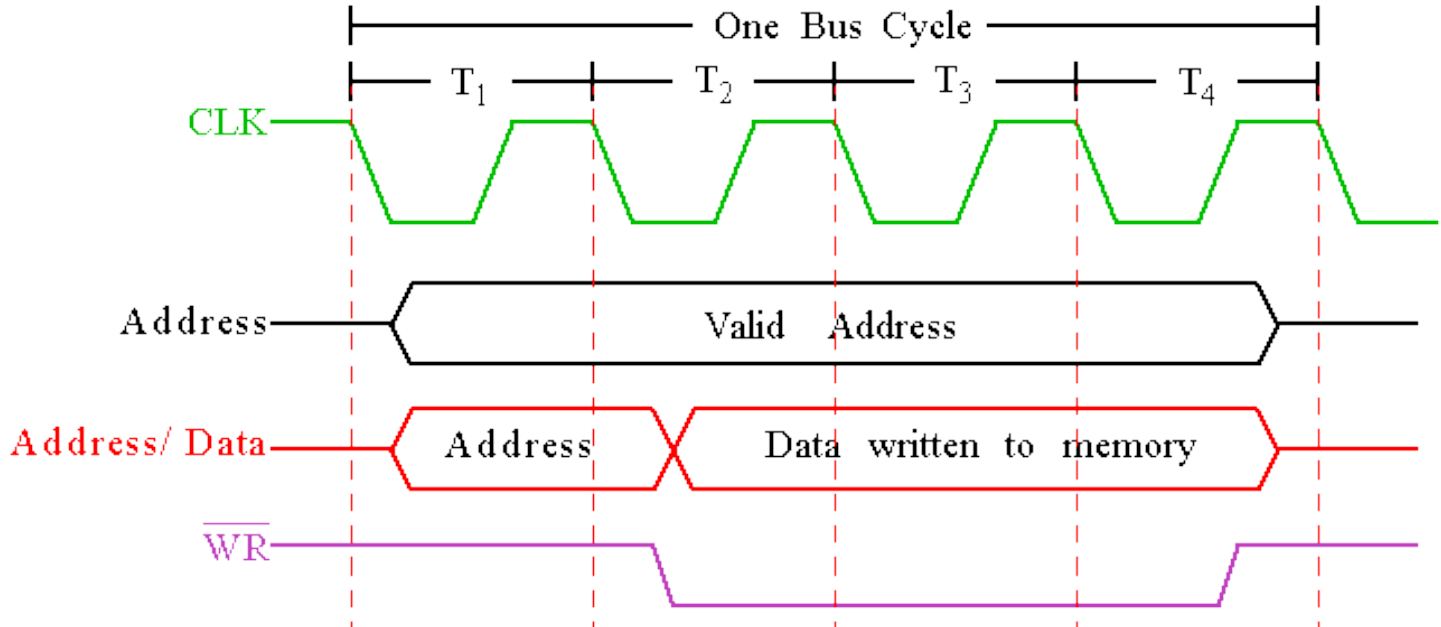
8.7 Bus Cycle and Time States

A bus cycle defines the basic operation that a microprocessor performs to communicate with external devices.

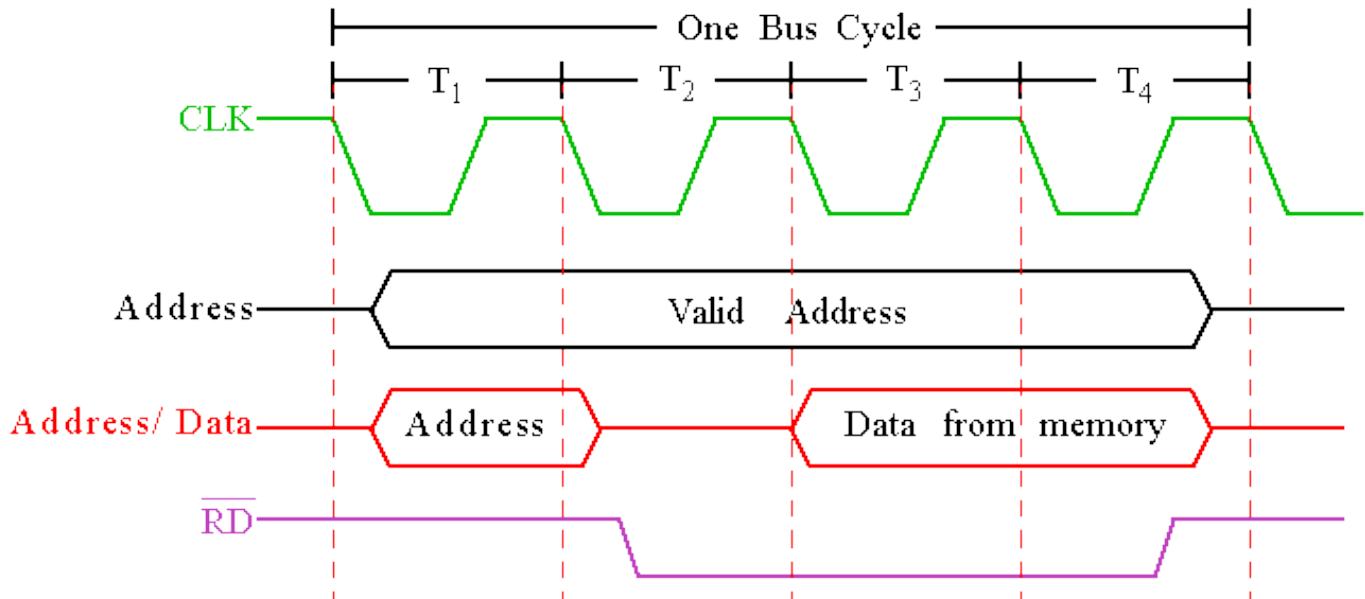
Examples of bus cycles are the memory read, memory write, input/output read, and input/output write.

The bus cycle of the 8088 and 8086 microprocessors consists of at least **four clock periods**. If no bus cycles are required, the microprocessor performs what are known as **idle states**. When READY is held at the 0 level, wait states are inserted between states T3 and T4 of the bus cycle.

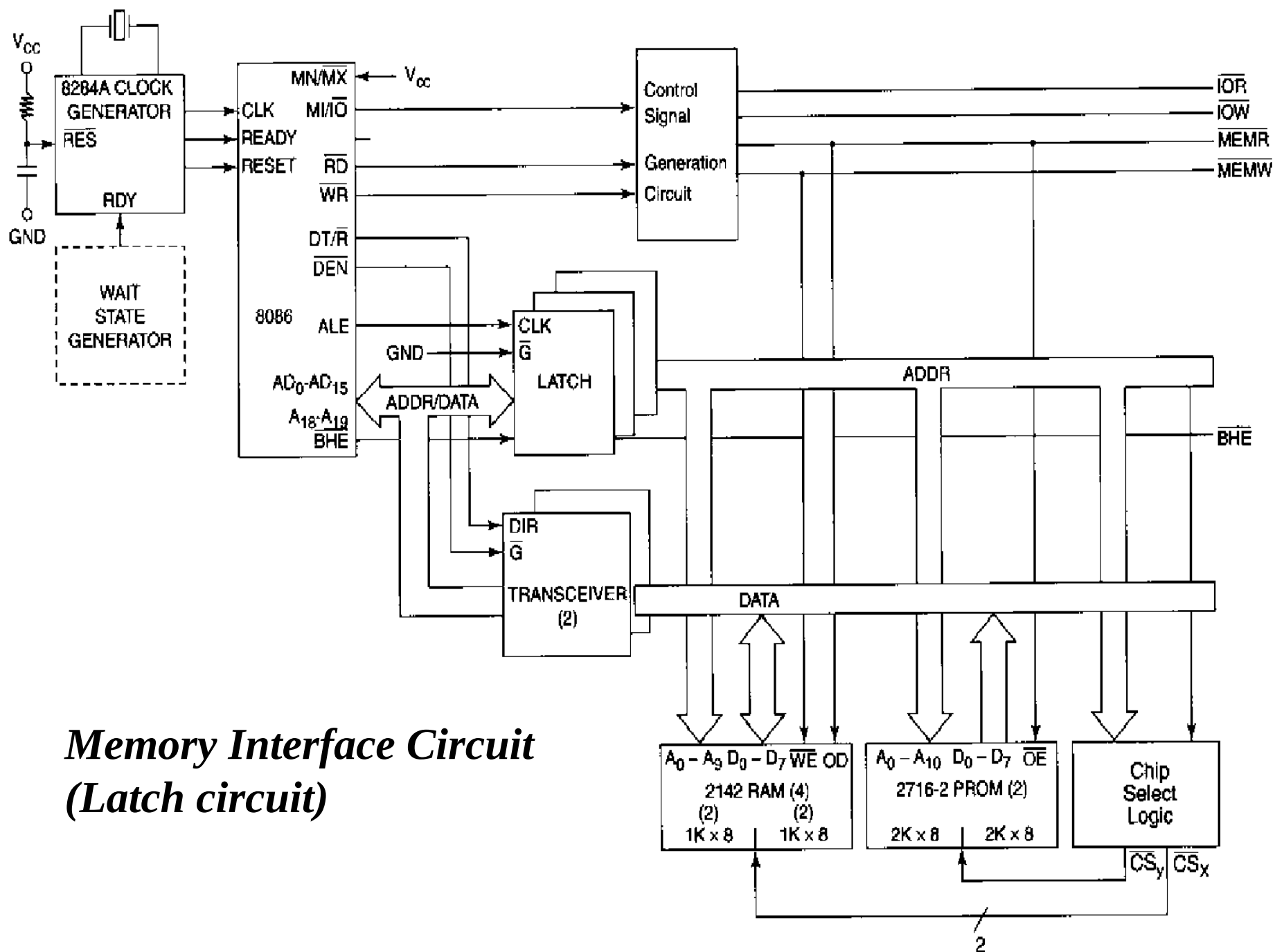
Bus Cycle:



Simplified 8086 Write Bus Cycle

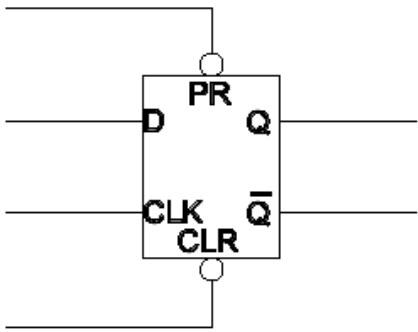


Simplified 8086 Read Bus Cycle

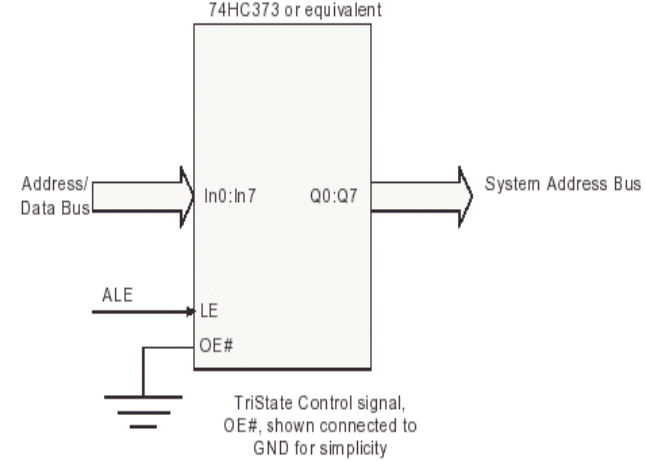


**Memory Interface Circuit
(Latch circuit)**

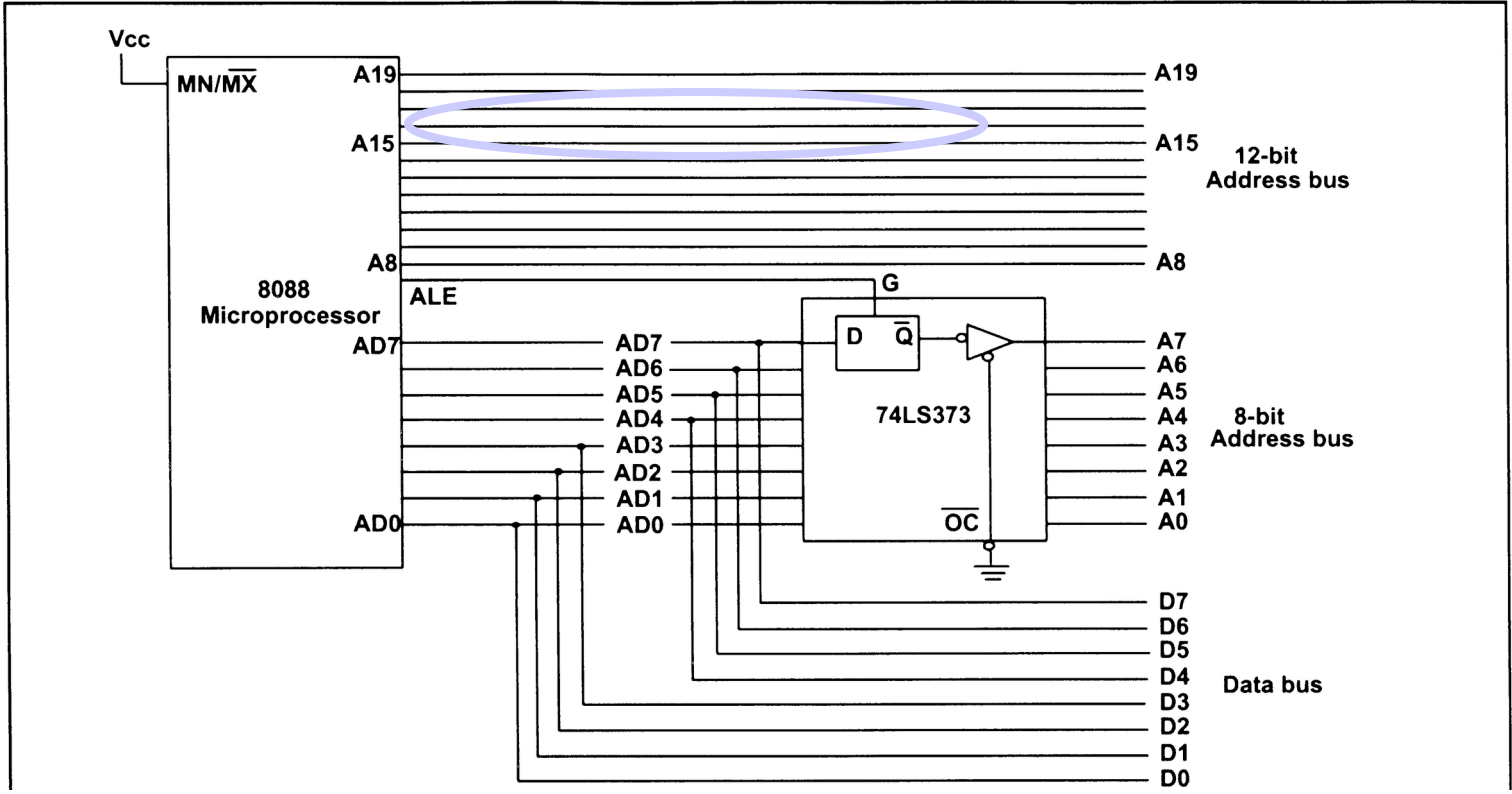
Adress latching:



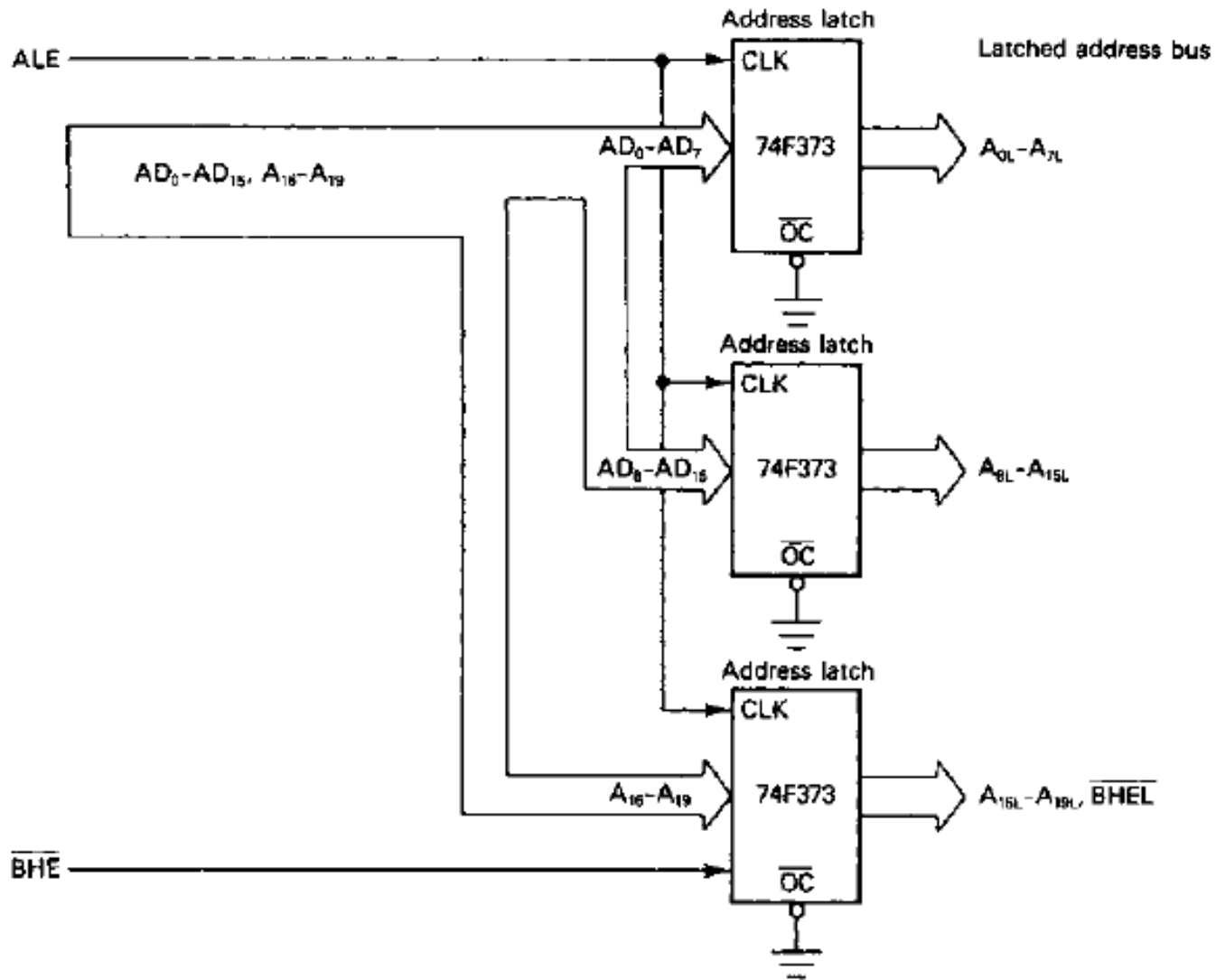
- D: Synchronous Data Input
- CLK: Clock Input
- Q: State Output
- Q-: Complemented Output
- PR: Asynchronous Preset Input
- CLR: Asynchronous Clear Input



Using the 74LS373 Address Latch



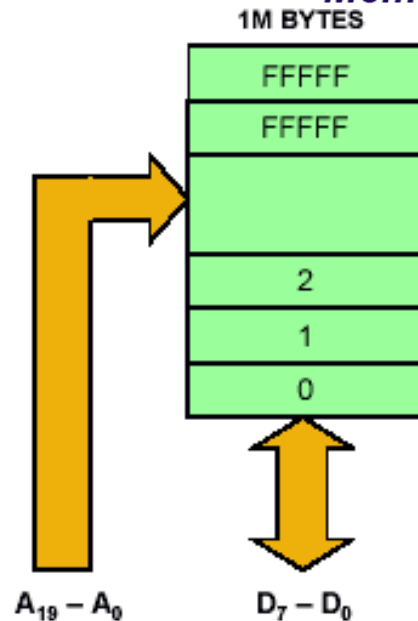
Memory Interface Circuit (Latch circuit)



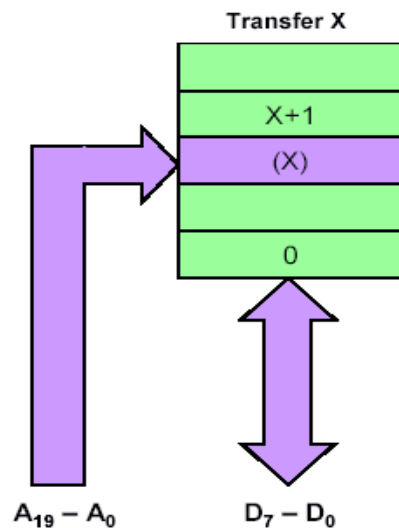
Before a memory can be interfaced to the microprocessor, the pin connections on the memory must be understood so they can be properly connected to the microprocessor's address, data, and control bus signals. Recall from the last note that the address bus contains the memory address to select a location in the memory or I/O. It then sends the control signals to cause a read ($\overline{RD}=0$) or a write ($\overline{WR}=0$) and to select memory ($IO/\overline{M}=0$) or I/O ($IO/\overline{M}=1$). Finally data, from the data bus, are written to the memory or I/O or read from the memory or I/O. In other words, see chart below!

<i>Operation</i>	$\overline{RD}$	$\overline{WR}$	$IO/\overline{M}$
Memory Read	0	1	0
Memory Write	1	0	0
I/O Read	0	1	1
I/O Write	1	0	1

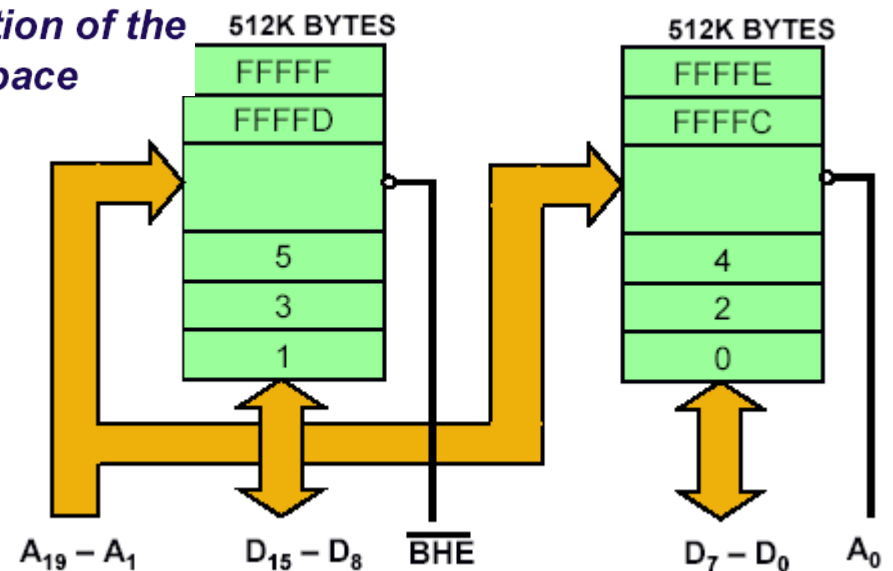
Hardware Organization of the Memory Address Space



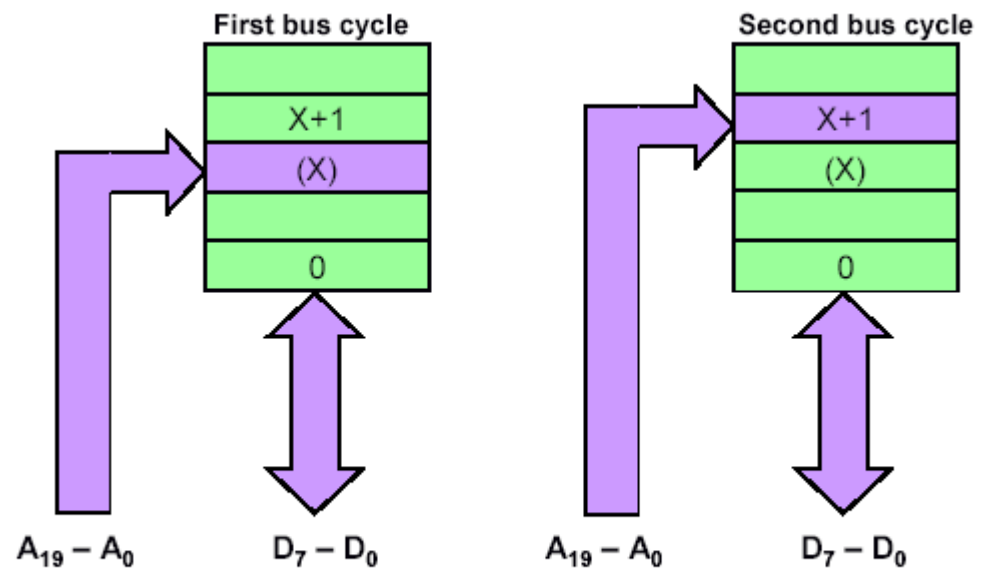
1Mx8 memory bank of the 8088



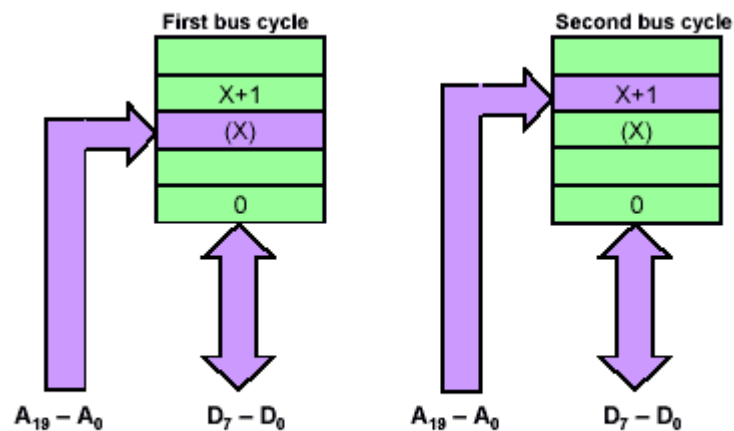
Byte transfer by the 8088



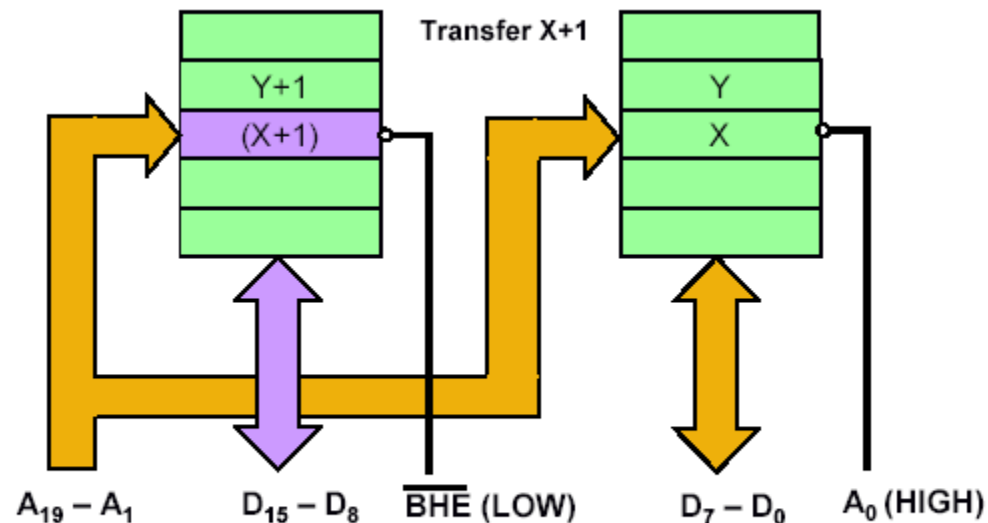
High and low memory banks of the 8086



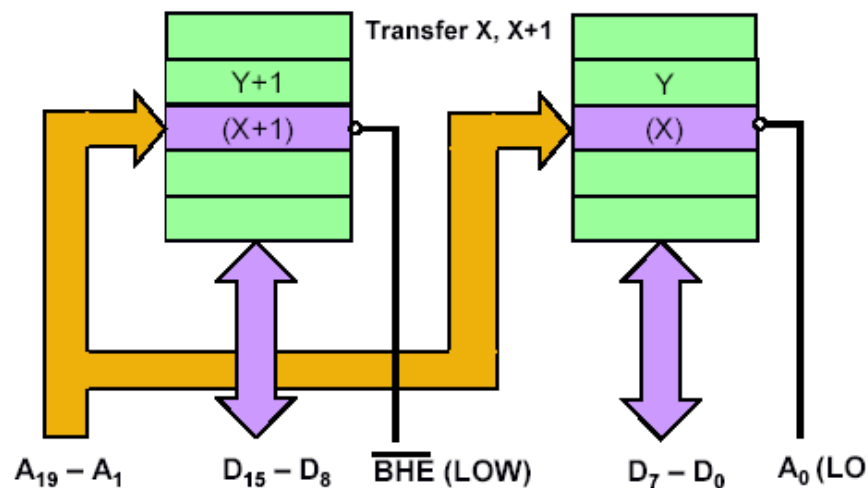
Word transfer by the 8088



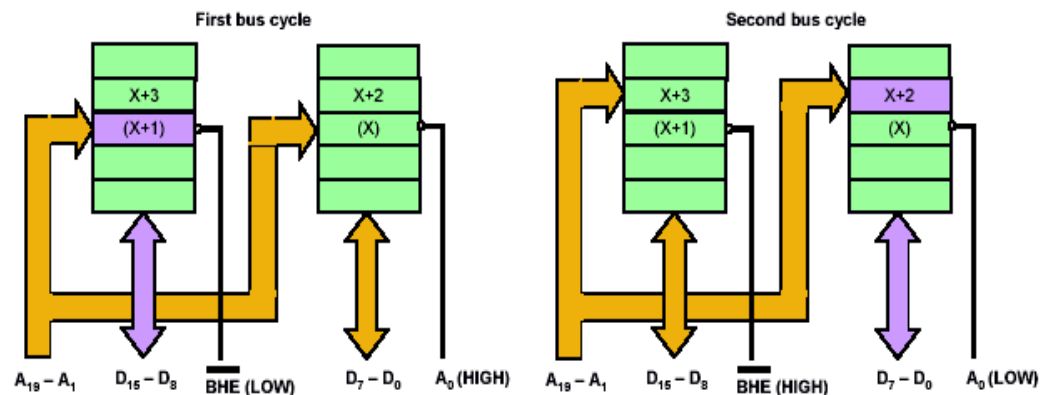
Word transfer by the 8088



Odd address byte transfer by the 8086



Even address word transfer by the 8086



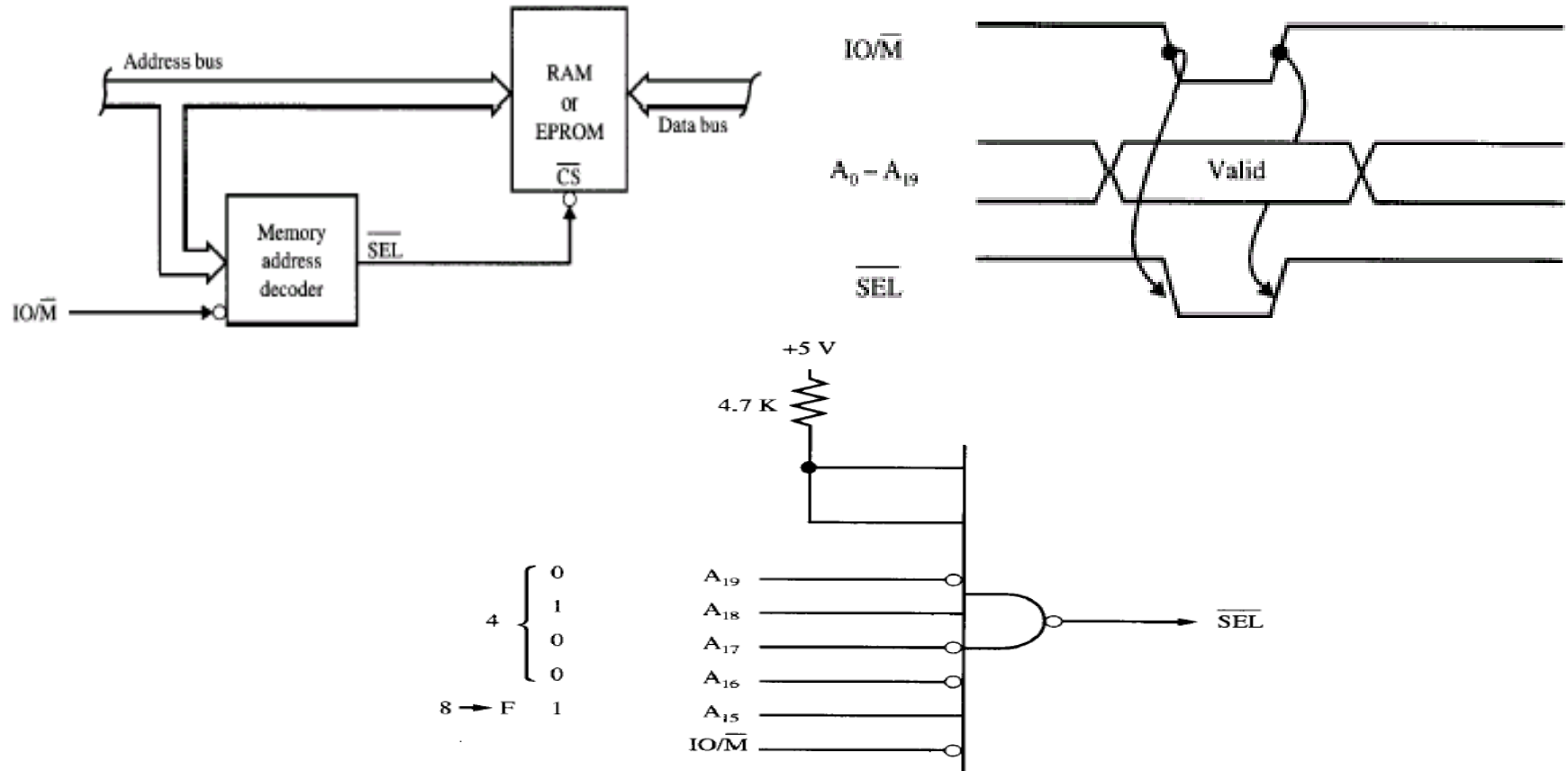
Odd-address word transfer by the 8086

Address decoding

CPU may interface with a number of memory ICs.

During a read/write operation, only the chip that stores the wanted data is enabled while the others are not.

Memory address decoding is to monitor the address bus and accordingly determine which of the memory chips is enabled.



Address decoding: basic techniques

Each memory chip is responsible for a section of the memory space, which contains a number of locations.

The higher bits of the address bus are used to select the chip while the lower bits identify the exact location in the chip.

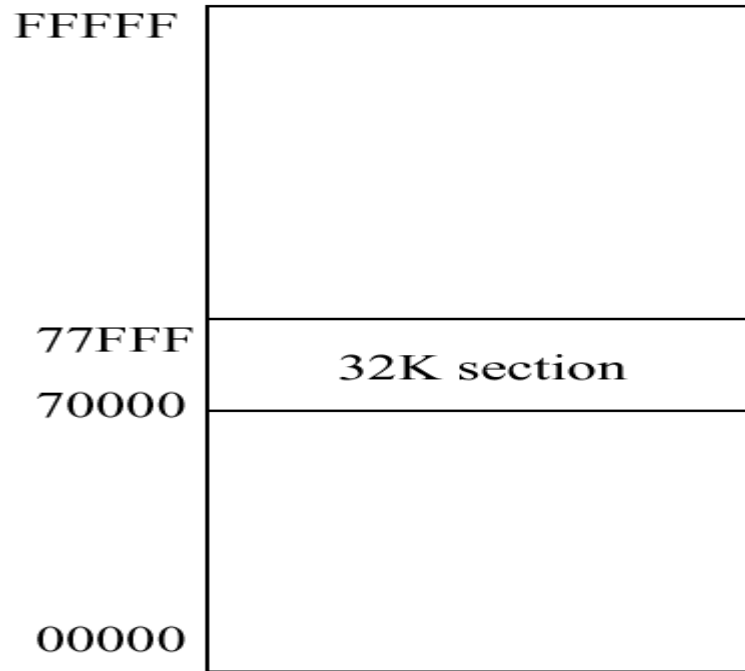
For a 32 KB RAM device, 15 address lines are needed for accessing all of the 32 K locations in the chip.

In this case, A0 to A14 go directly into the RAM. A15 through A19 are used to determine where the 32 KB block is located in the entire 1 MB memory space.

If the RAM starts from address 48000H, the 20-bit address for any location in this chip must be

0100 1xxx xxxx xxxx xxxx

Memory Map



For 32 K byte chip

$$70000 = 0111\ 0000\ 0000\ 0000\ 0000$$

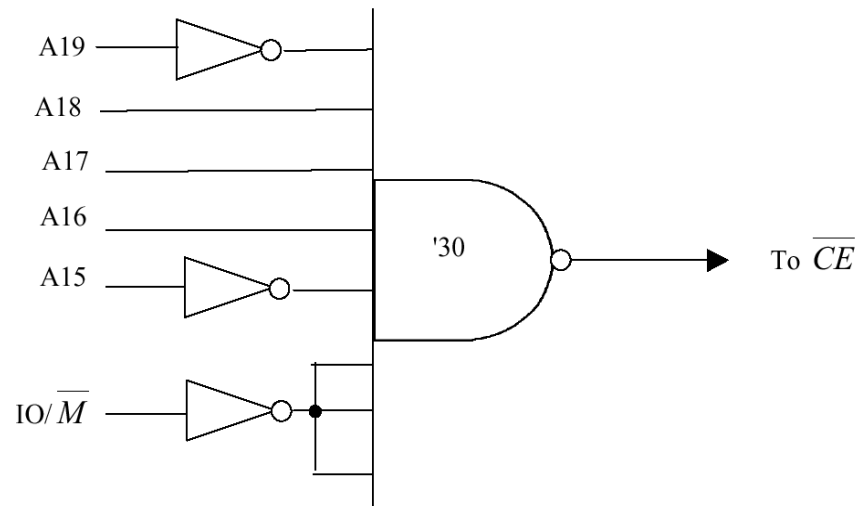
$$77FFF = 0111\ 0111\ 1111\ 1111\ 1111$$

(A0–A14)

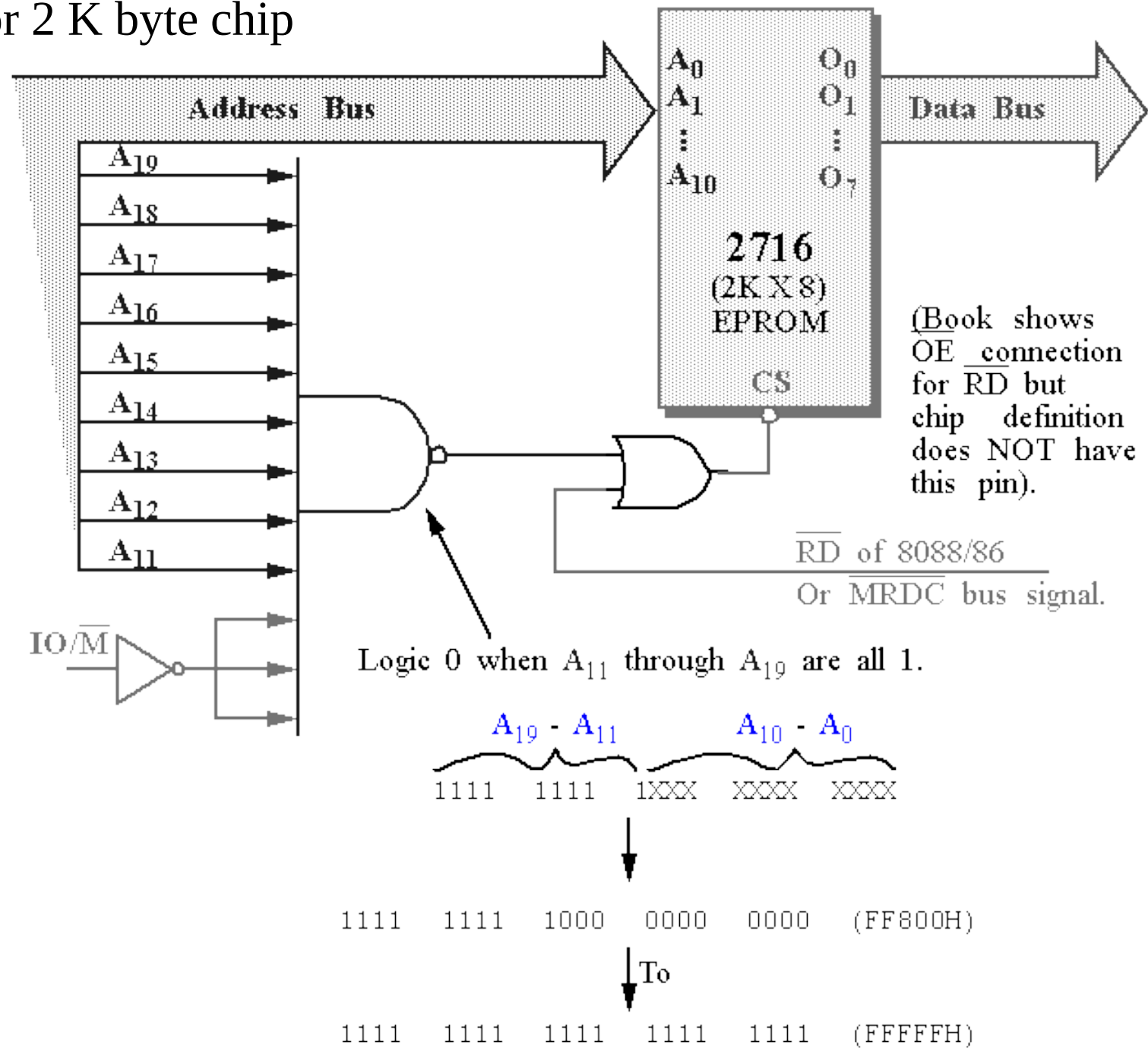
$$70000 = 0111\ 0000\ 0000\ 0000\ 0000$$

$$77FFF = 0111\ 0111\ 1111\ 1111\ 1111$$

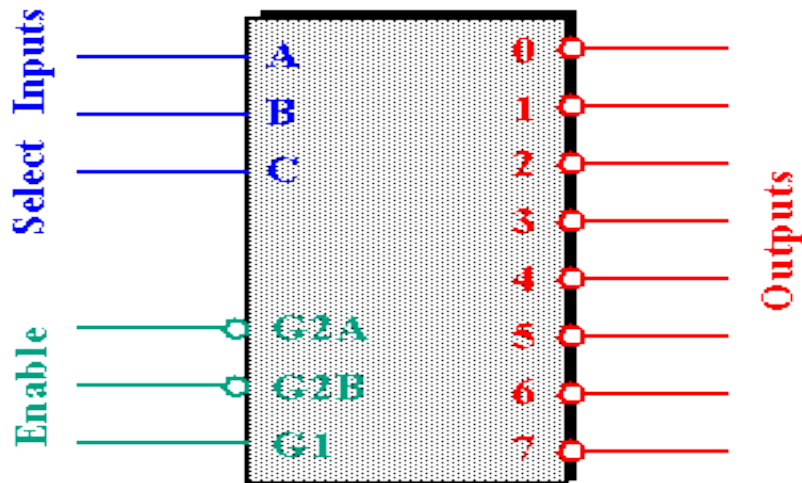
0111 0 ← remaining bits!



For 2 K byte chip



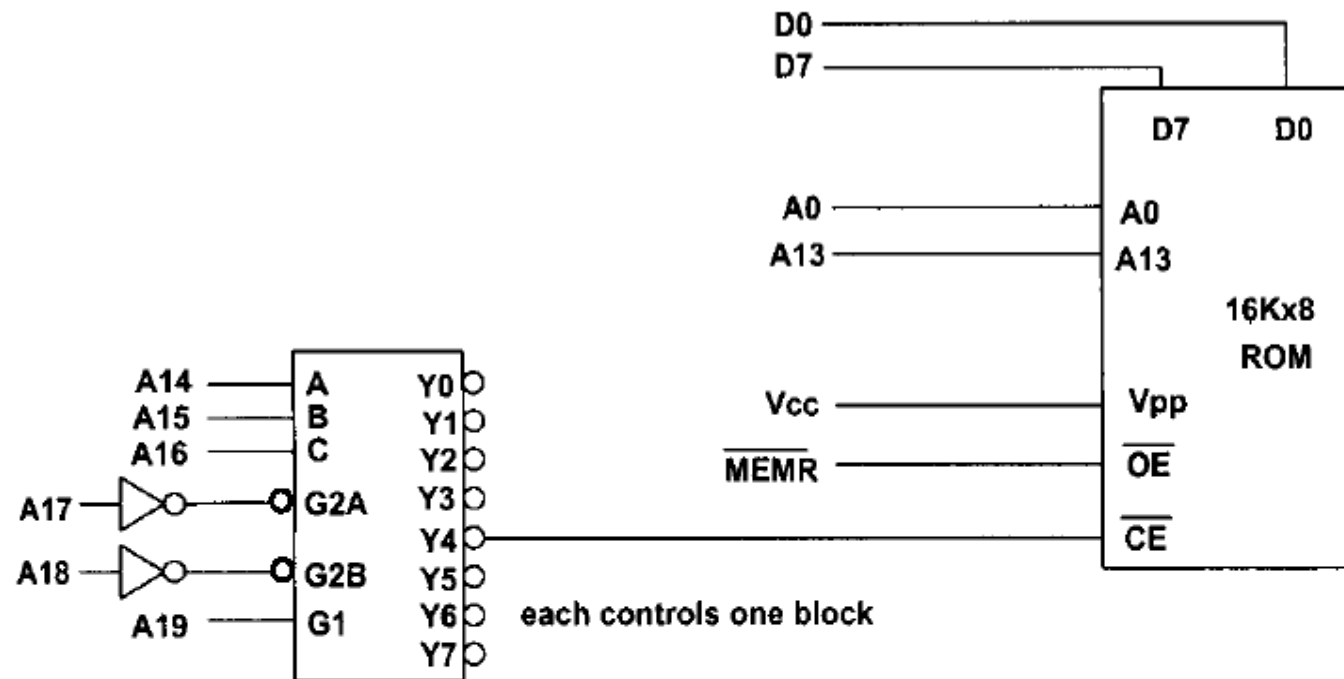
74LS 3x8 decoder chip



Inputs						Output							
Enable			Select										
G2A	G2B	G1	C	B	A	0	1	2	3	4	5	6	7
1	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	0	X	X	X	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0

- Note that all three Enables (G2A, G2B, and G1) must be active, e.g. low, low and high, respectively.
- Each output of the decoder can be attached to an 2764 EPROM (8K X 8).

Address decoding using 74LS138



This decoder is functioning only when $A17 = 1$, $A18 = 1$ and $A19 = 1$.

That is, addresses being accessed are

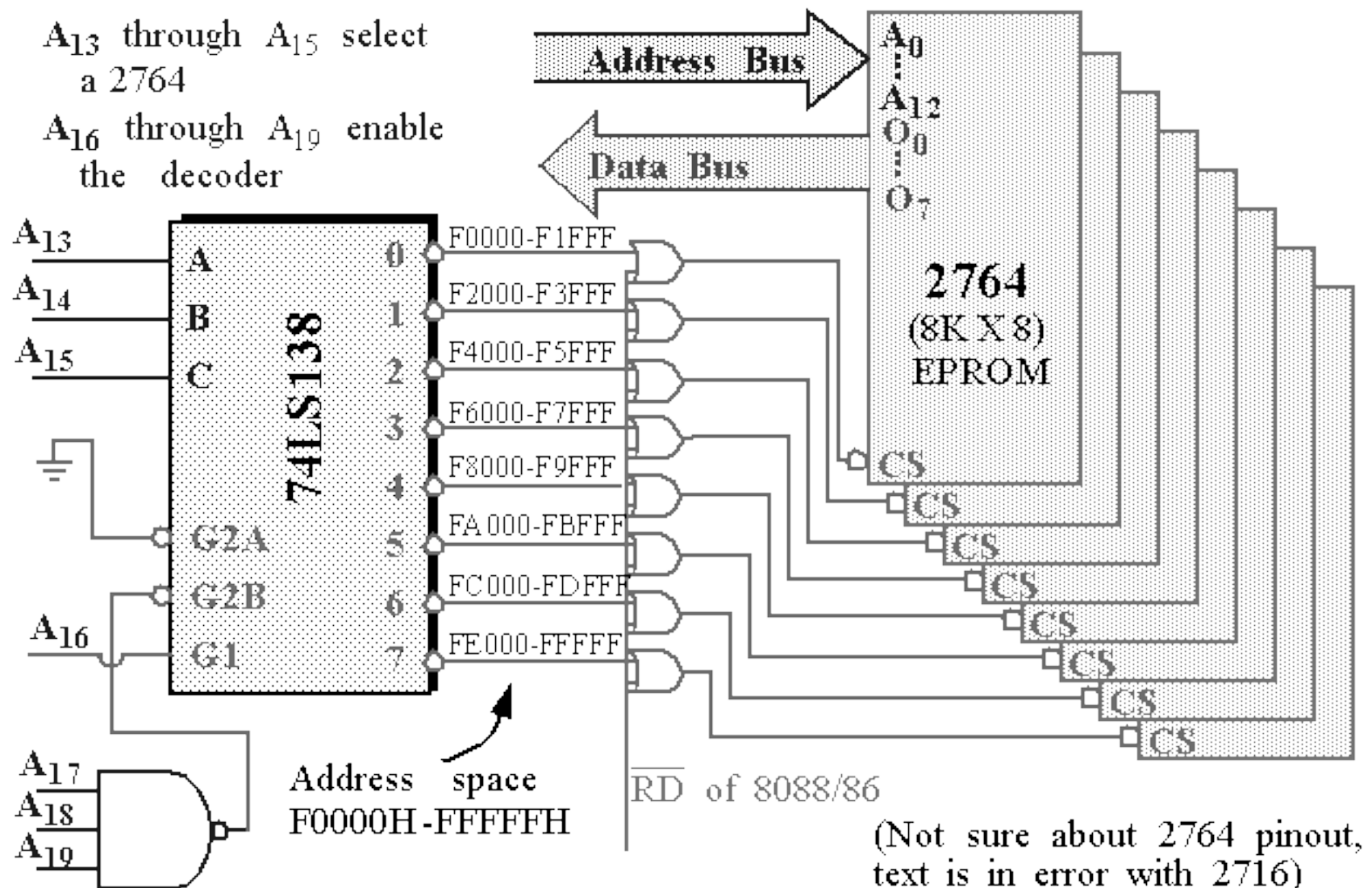
111y yyxx xxxx xxxx xxxx

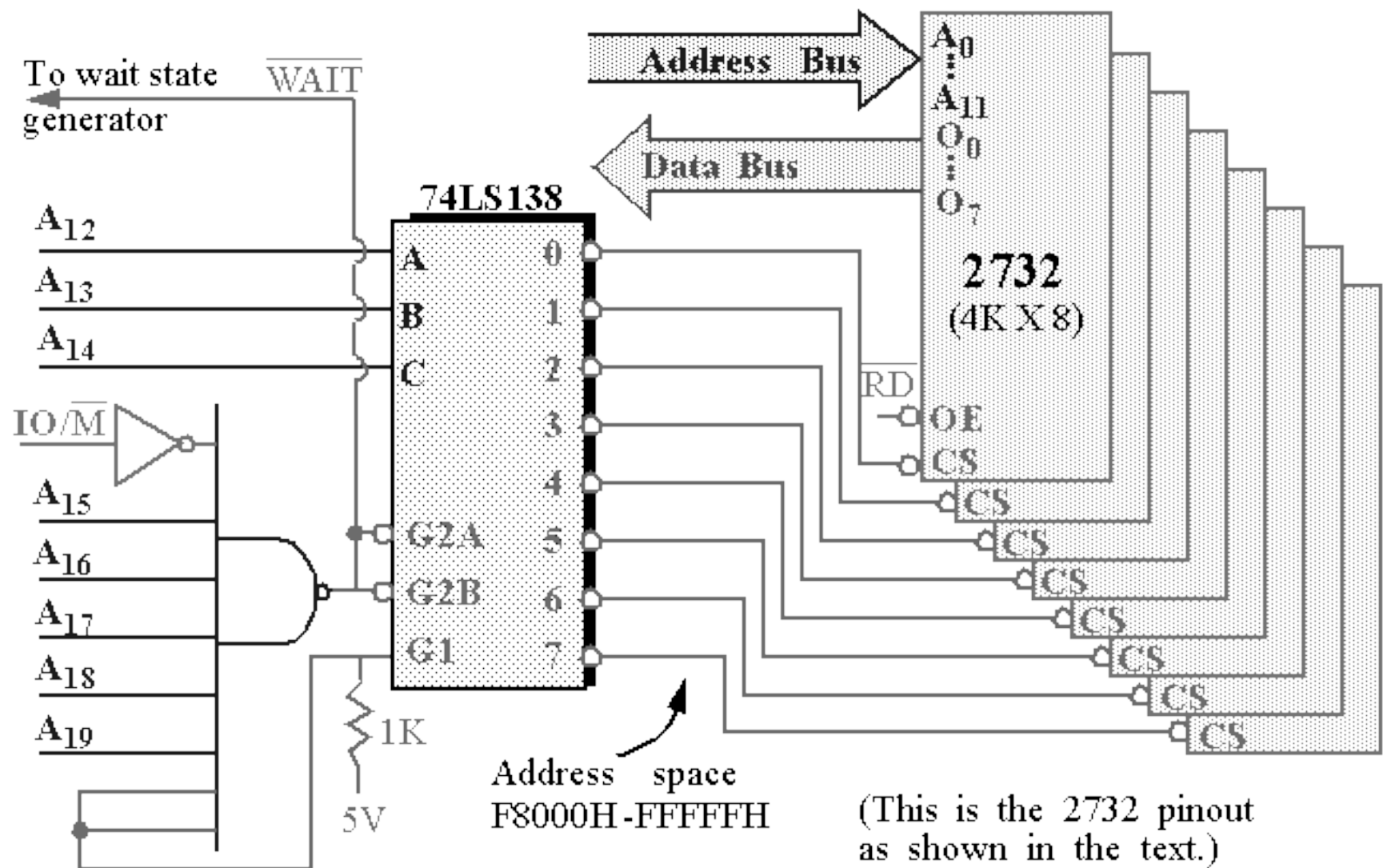
where the “yyy” are from A14 - A16. A0 - 13 are used to select the exact location within a memory chip.

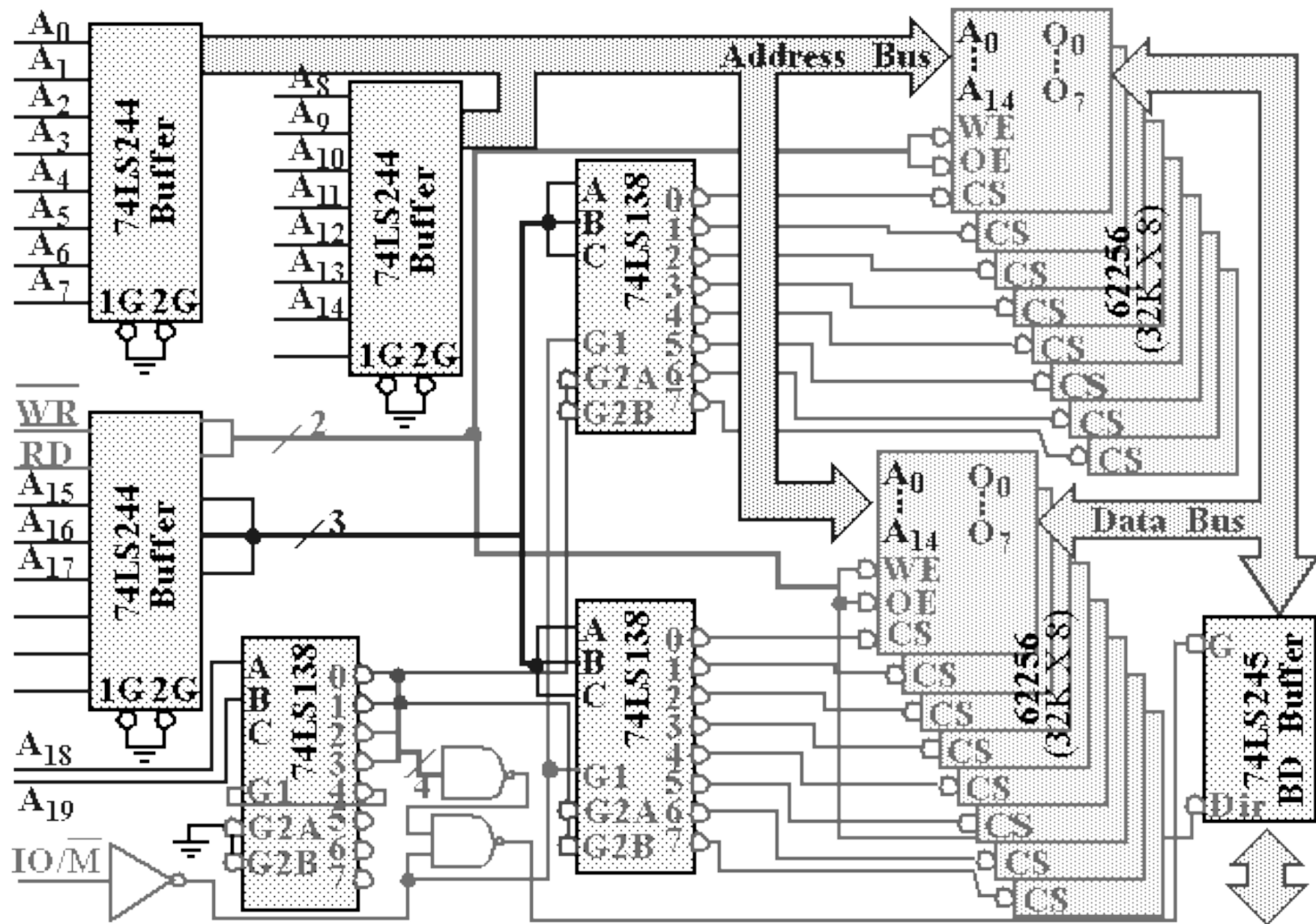
In this example, Y4 is low when $A14 = 0$, $A15 = 0$ and $A16 = 1$. Thus the corresponding address range is F0000H - F3FFFH.

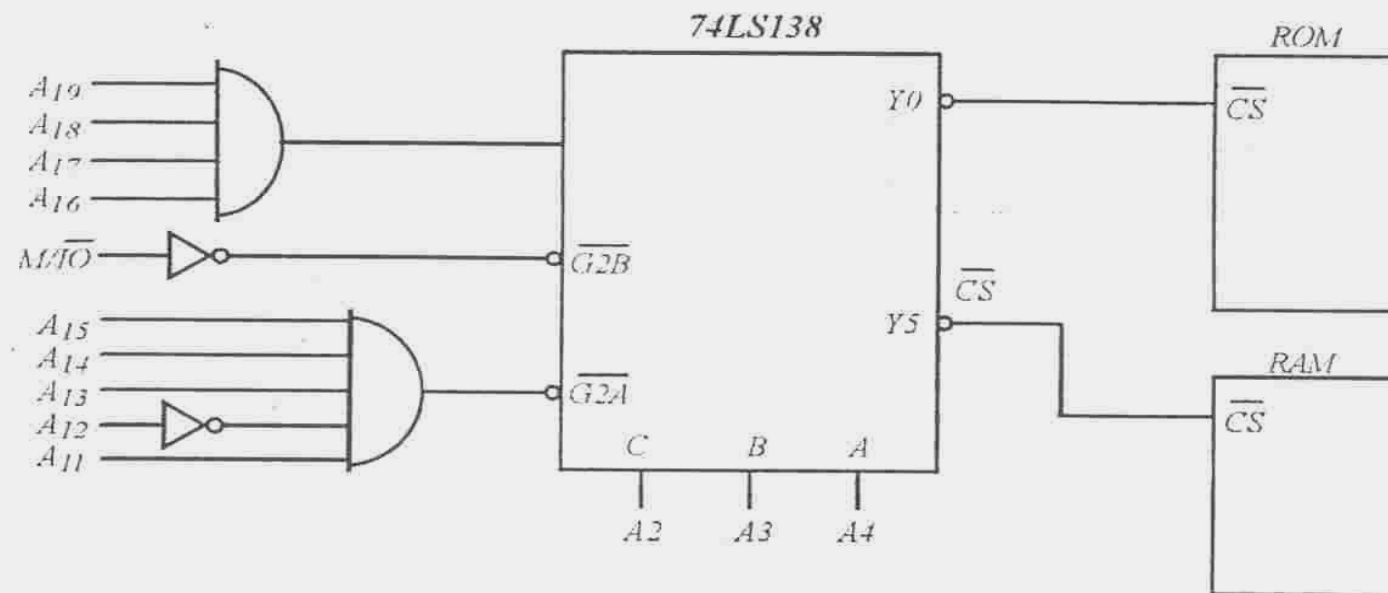
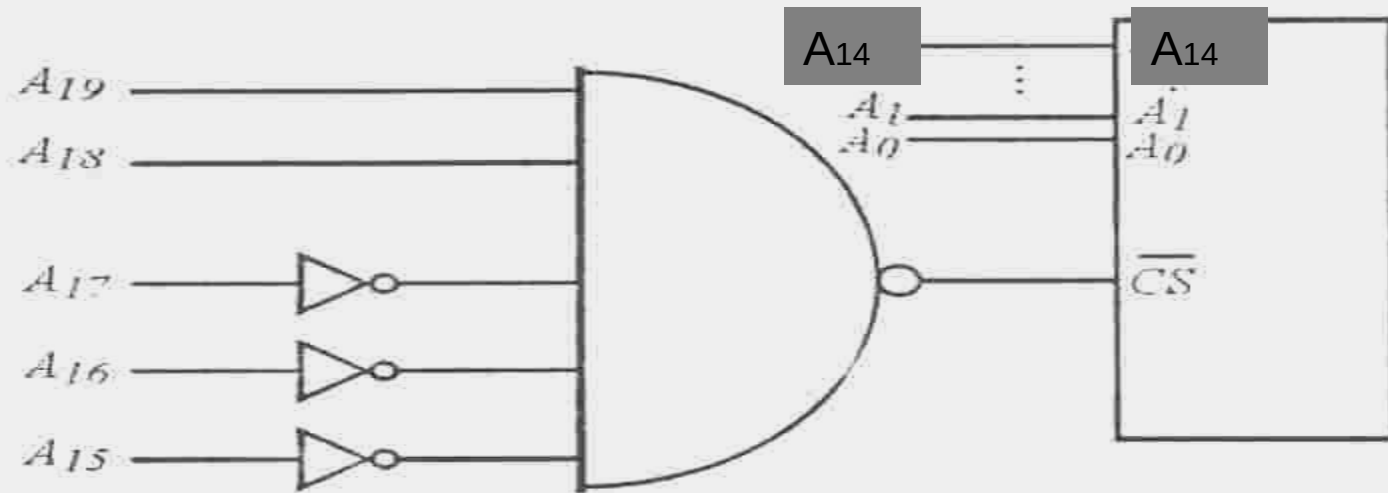
A_{13} through A_{15} select
a 2764

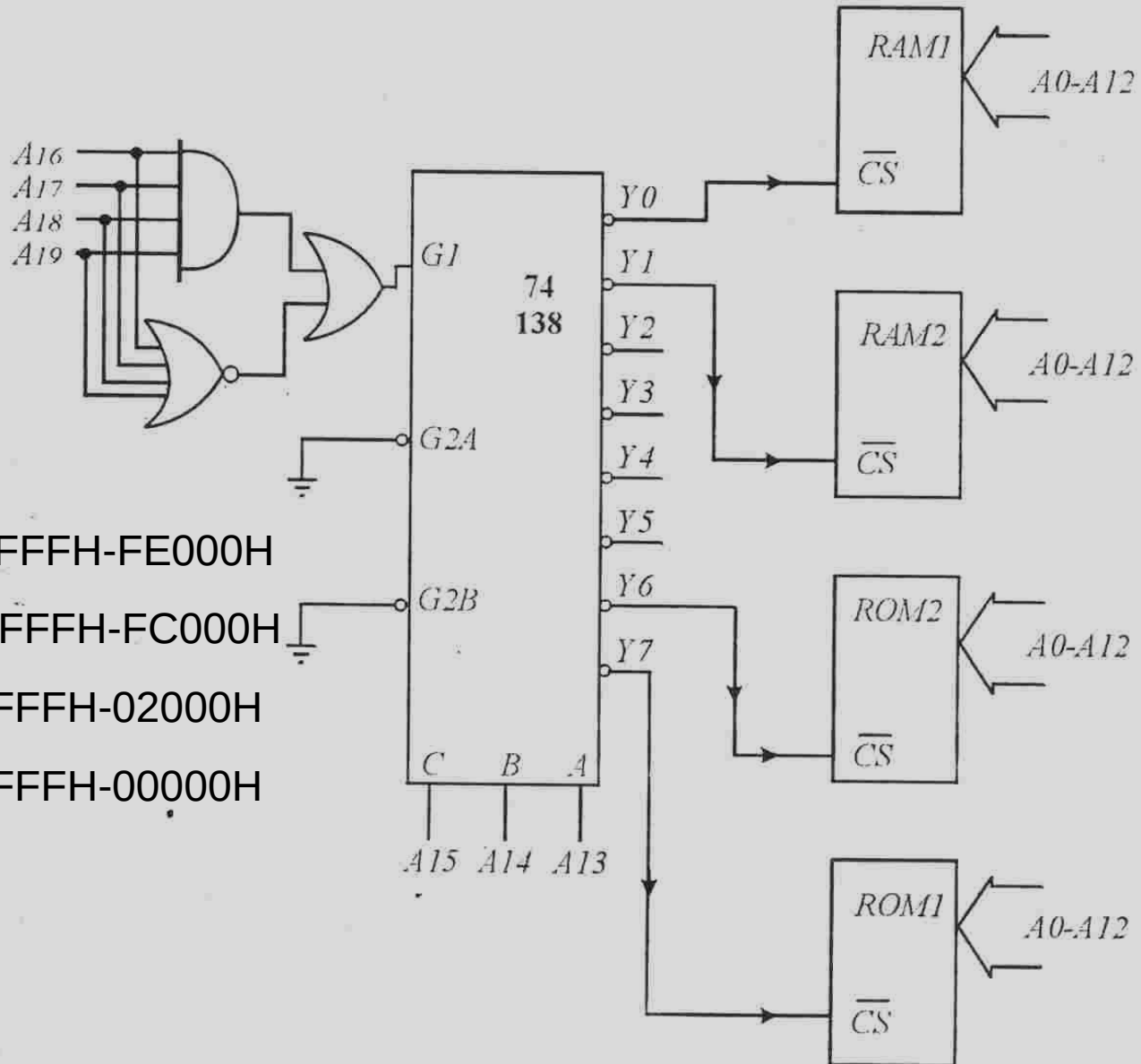
A_{16} through A_{19} enable
the decoder











Rom1 FFFFFH-FE000H

Rom1 FDFFFH-FC000H

Ram2 03FFFH-02000H

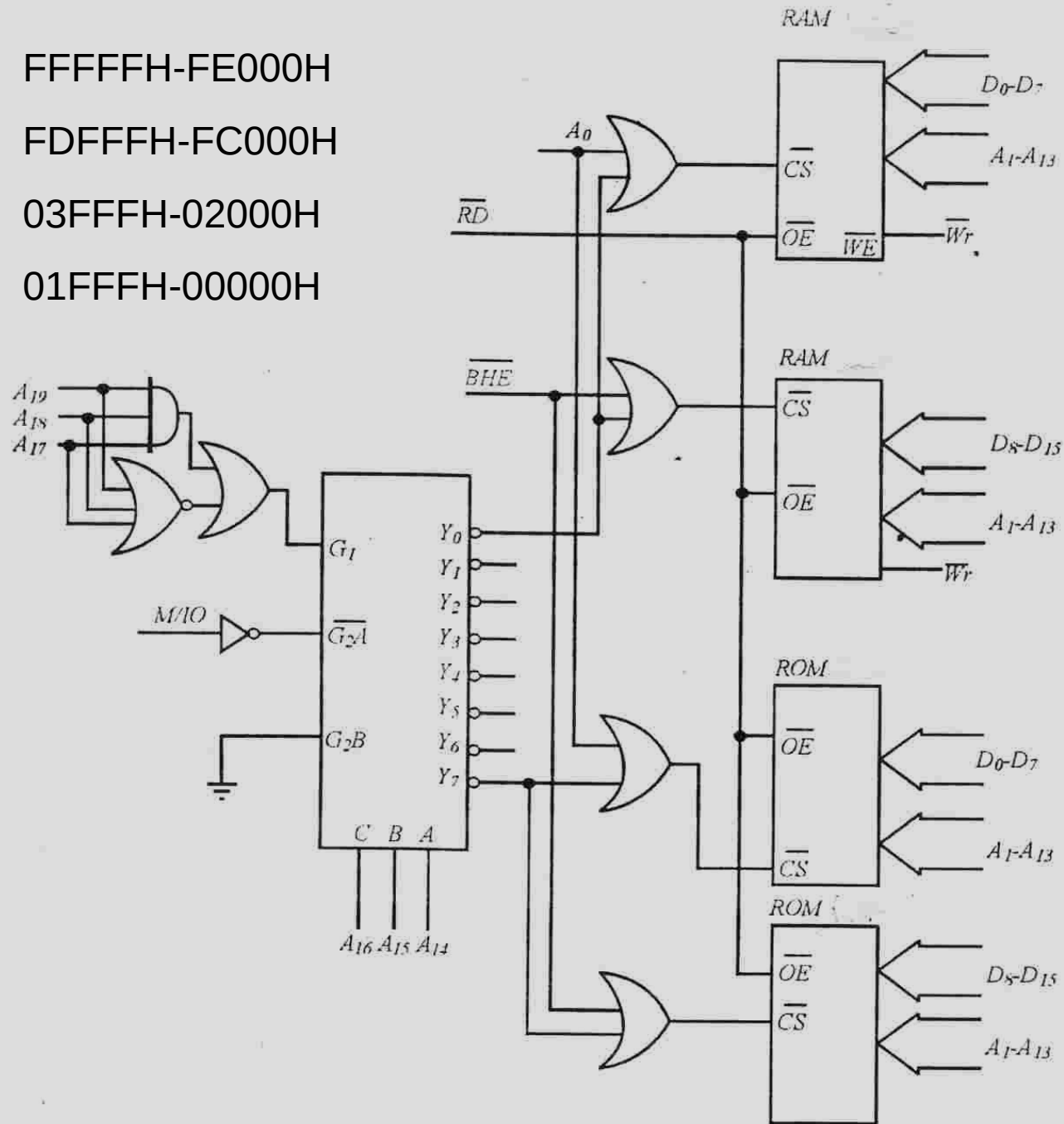
Ram1 01FFFH-00000H

Rom1 FFFFFH-FE000H

Rom1 FDFFFH-FC000H

Ram2 03FFFH-02000H

Ram1 01FFFH-00000H



4 ROM memory and
4 RAM memory chip
are used for total
memory . Each
memory chip is 2
kbyte

A0 and A10 are
used as adress bus

IC1.....IC4 Ram

IC5,.....IC8 ROM

