

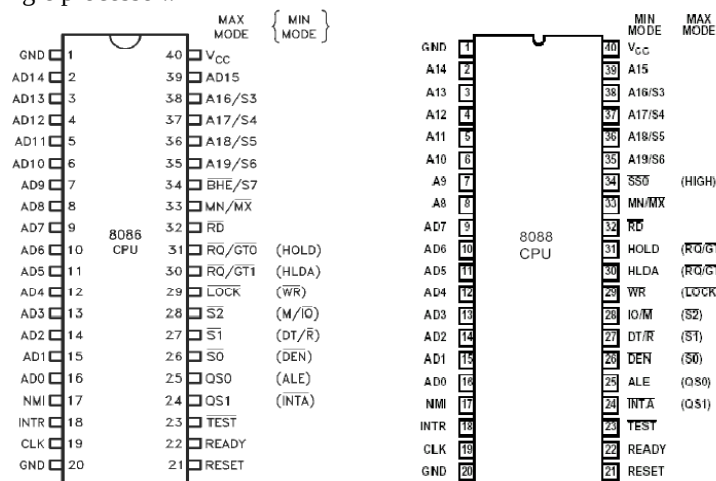
# EEM332 Lecture7: Hardware of 8086 based system Address bus, Data Bus, Control Bus Memory design, Address decoding

## 8086 Hardware design

The 8086 and 8088 microprocessors can be configured to work in either of two modes:

The minimum mode - The maximum mode -

The mode selection feature lets the 8088 or 8086 better meet the needs of a wide variety of system requirement. Minimum mode 8088/8086 systems are typically smaller and contain a single processor..



Note: that for 8088 the address bus is 20 bit and data bus is 8-bit.

### System Clock

The time base for synchronization of the internal and external operations of the microprocessor in a microcomputer system is provided by the *clock* (CLK) input signal.

The standard 8088 operates at 5 MHz and the 8088-2 operates at 8 MHz.

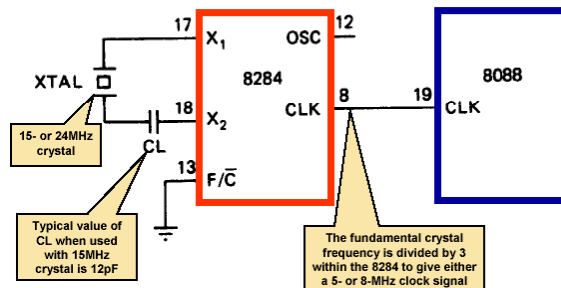
The 8086 is manufactured in three speeds: 5-MHz

8086, 8-MHz 8086-2, and the 10-MHz 8086-1.

**The CLK is externally generated by the 8284 clock generator and driver IC.**

### System Clock

Connecting the 8284 to the 8088



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### Pin Descriptions of the Control Signals of 8086 CPU

| Pin | Name                                                    | Function                                                                                                                                                                                          |
|-----|---------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 34  | $\overline{\text{BHE}}$ (Bus High Enable)               | It provides control signal to distinguish between the low byte and the high byte of the 16-bit data. (Active-low)                                                                                 |
| 17  | $\text{NMI}$ (Nonmaskable Interrupt)                    | This signal will make the microprocessor to jump to the interrupt vector table after it finishes the current instruction. This interrupt cannot be masked by software.                            |
| 18  | $\text{INTR}$ (Interrupt Request)                       | If it is activated, it will finish the execution of the current instruction and respond with the interrupt acknowledge operation. In IBM PC it is connected to the interrupt controller.          |
| 19  | $\text{CLK}$ (Clock)                                    | It acts as the heartbeat of the CPU. Intel has designed the 8284 clock generator and a driver to be used for the processor.                                                                       |
| 21  | $\text{RESET}$                                          | To terminate the present activities of the microprocessor, a high signal is applied for the RESET pin.                                                                                            |
| 22  | $\text{READY}$                                          | It is an input signal used to insert a wait state for slower memories and I/O. It inserts wait states when it is low.                                                                             |
| 23  | $\overline{\text{TEST}}$                                | This is input from the 8087 coprocessor. During execution of a wait instruction, the CPU checks this signal. If it is low, execution of the signal will continue; if not, it will stop executing. |
| 24  | $\overline{\text{INTA}}$ (Interrupt acknowledge)        | Active-low output signal. Informs interrupt controller that INTR has occurred and that the vector number is available on the lower 8 lines of the data bus                                        |
| 25  | $\text{ALE}$ (Address Latch Enable)                     | Active-high output signal. Indicates that a valid address is available on the external address bus. See Figure 9-3.                                                                               |
| 26  | $\overline{\text{DEN}}$ (Data Enable)                   | Active-low output signal. This allows the isolation of the CPU from the system bus.                                                                                                               |
| 27  | $\text{DT}/\overline{\text{R}}$ (Data transmit/receive) | Active-low output signal used to control the direction of the data flow (transmit/receive)                                                                                                        |

|    |                                                          |                                                                                                                                                                                      |
|----|----------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 28 | $\text{IO}/\overline{\text{M}}$ (memory or input/output) | Indicates whether the address bus is accessing memory or I/O device. In 8086, when it is high, it is accessing the memory and when it is low, it is accessing the I/O.               |
| 29 | $\overline{\text{WR}}$ (Write)                           | Active-low output signal. Indicates that the data on the data bus is being written to memory or I/O. Used along with pin 28 for write operations.                                    |
| 30 | $\text{HLDA}$ (hold acknowledge)                         | Active-high output signal. After input on HOLD, the CPU responds with HLDA to signal that <b>DMA (Direct Memory Access)</b> controller can use the bus.                              |
| 31 | $\text{HOLD}$ (hold)                                     | Active-high input from the DMA controller which indicates that the device is requesting access to memory and I/O space and that the CPU should release the control of the local bus. |
| 32 | $\overline{\text{RD}}$ (Read)                            | Active-low output signal. Indicates that the data on the data bus is being read from the memory or I/O. Used along with pin 28 for read operations.                                  |

**RESET** : Microprocessor resets if this pin is held high for 4 clock periods.

### Direct Memory Access (DMA)

To transfer a large amount of data between the memory and peripherals such as hard disk. In such a case using the CPU to transfer data is too slow, since the data first must be fetched into the CPU and then sent to its destination. For this reason Direct Memory Access controller is used to bypass the CPU and provide a direct connection between the peripherals and memory, thus transferring the data as fast as possible.

#### Basic Busses for a computer:

Every computer must have three basic busses in order to communicate: Address bus, data bus, and the control bus. The figure below shows the basic busses of 8088 based-computer. Note that the 3 control signals from 8088:  $\overline{\text{WR}}$ ,  $\overline{\text{RD}}$ , and  $\text{IO}/\overline{\text{M}}$  are used to generate 4 new control signals ( $\text{MEMR}$ ,  $\text{MEMW}$ ,  $\text{IOR}$ , and  $\text{IOW}$ ) by using a decoder circuit.

### Pin descriptions of 8086 Microprocessor

**Data Bus:** - In 8086 microprocessor Pins AD0 – AD15 are used for the data bus.

- However the same pins are also used for Address bus as well.

- The ALE (Address Latch Enable –pin 25) signals whether the information on pins AD0 – AD15 is used address or data.

- When the data is sent out or in, the case when ALE is low indicates that AD0-AD15 will be used as data bus.

- When the address data is sent out, the ALE is high indicating that AD0-AD15 will be used as address bus, - This process of separating address and data from pins AD0-AD15 is called demultiplexing.

**Address Bus:** - The 8086 CPU has 20-bit address bus, where the AD0-AD15 and A16-A20 are used as the address bus. To demultiplex the address signals from the address/data pins (AD0-AD15) a latch must be used to grab the addresses.

- In 8086 microprocessor the address bus is 20-bit wide, however only 16-bit is shared with data bus (AD0-AD15) through demultiplexing. The most widely used latch for demultiplexing is 74LS373 IC

**-Control Bus : is used to indicate**

- When a valid address is on the address bus

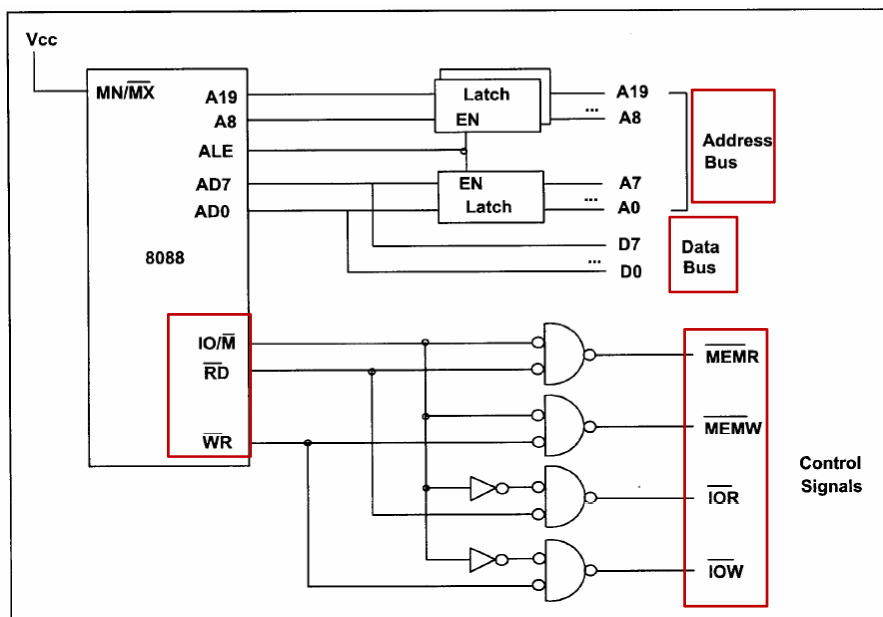
- In which direction data are to be transferred over the data bus (in/out)

- When external devices can read/write data on the data bus.

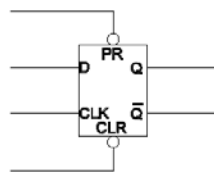
- When valid read/write data are on the data bus.

- Etc.

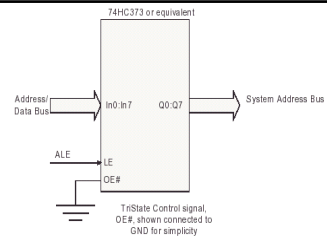
### Address, Data and control Buses



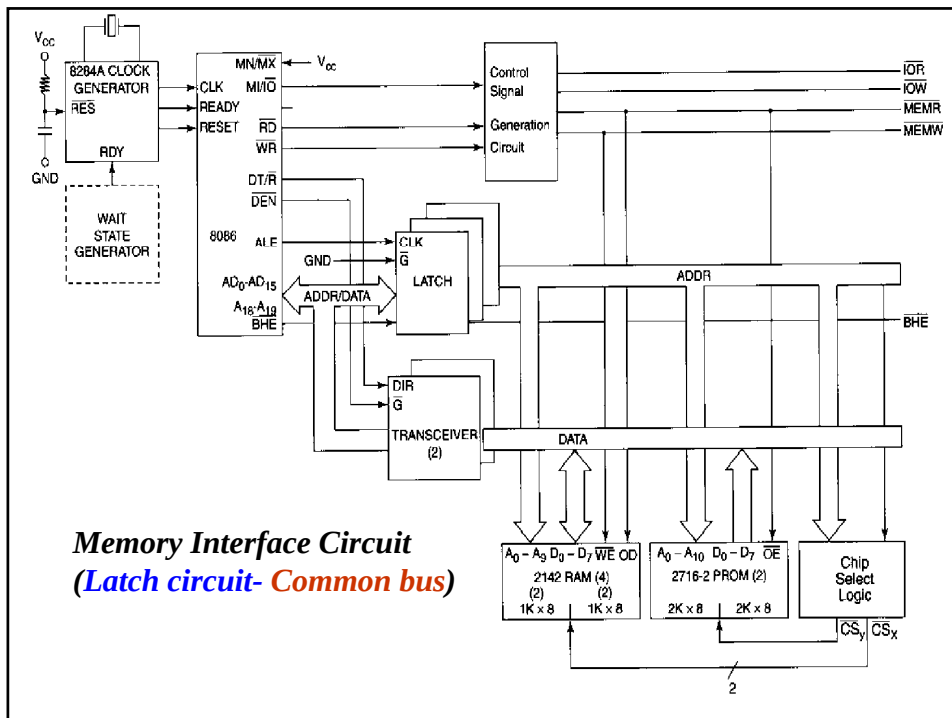
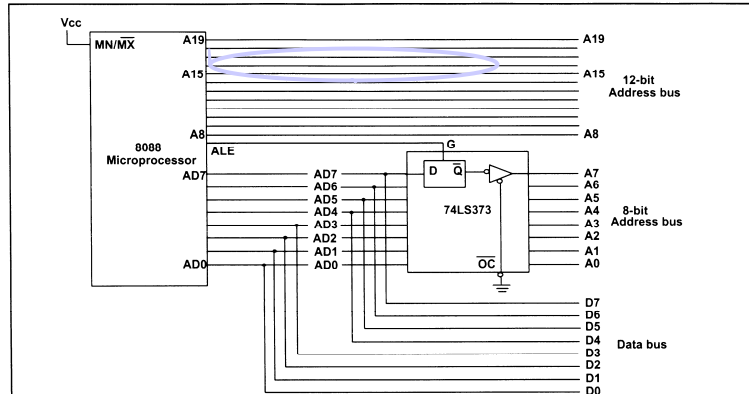
## Address latching:



**D:** Synchronous Data Input  
**CLK:** Clock Input  
**Q:** State Output  
**Q-:** Complemented Output  
**PR:** Asynchronous Preset Input  
**CLR:** Asynchronous Clear Input



## Using the 74LS373 Address Latch



**Memory** In the design of all computers, semiconductor memories are used as primary storage for data and code.

- They are connected directly to the CPU and they are the memory that the CPU asks for information (code or data)
- Among the most widely used are RAM and ROM
- **Memory Capacity**
  - The number of bits that a semiconductor memory chip can store is called its chip capacity (bits or bytes)
- **Memory Organization**
  - Each memory chip contains  $2^x$  locations where x is the number of address pins on the chip
  - Each location contains y bits, where y is the number of data pins on the chip
  - The entire chip will contain  $2^x * y$  bits
  - Ex. Memory organization of  $4K \times 4$ :  $2^{12} = 4096$  locations, each location holding 4 bits
- **Memory Speed** (access time)
- Each memory device has at least one **chip select (CS)** or **chip enable (CE)** or **select (S)** pin that enables the memory device.
  - This enables read and/or write operations.
- Each memory device has at least one **control** pin.
  - For ROMs, an **output enable (OE)** or **gate (G)** is present. The OE pin enables and disables a set of tristate buffers.
  - For RAMs, a **read-write (R/W)** or **write enable (WE)** and **read enable (OE)** are present

## Memory

### •ROM (Read Only Memory)

- ❖ ROM is the type of memory that does not lose its contents when power is turned off. It is also called **nonvolatile** memory.
- ❖ PROM (Programmable Memory)
  - User programmable (one-time programmable) memory
  - If the information burned into PROM is wrong, it needs to be discarded since internal fuses are blown permanently.
  - Special equipment needed: ROM burner or ROM programmer
- ❖ EPROM (Erasable Programmable ROM) 2,000 times
  - Allows making changes in the contents of PROM after it is burned
  - One can program the memory chip and erase it thousands of times
  - Erasing its contents can take up to 20 minutes; the entire chip is erased
  - All EPROM chips have a window that is used to shine ultraviolet (UV) radiation to erase its contents
  - Also referred to as UV-EPROM

## Memory

### ❖ EEPROM (Electrically Erasable ROM) 500,000 times

- Method of erasure is electrical
- Moreover, one can select which byte to be erased
- Cost per bit is much higher than for UV-EPROM

### ❖ Flash Memory EPROM

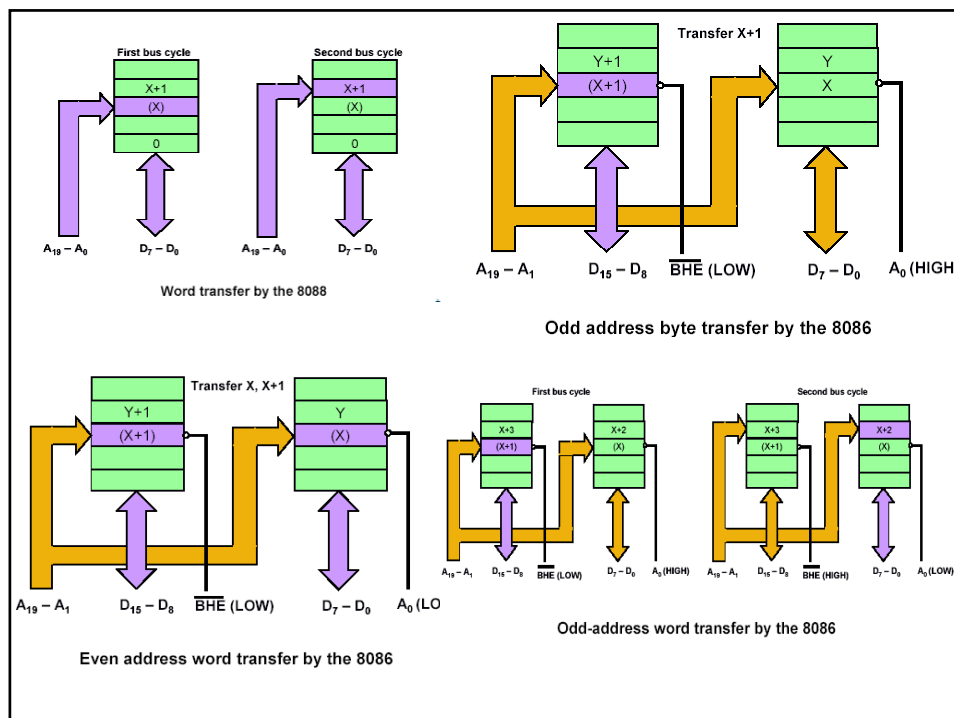
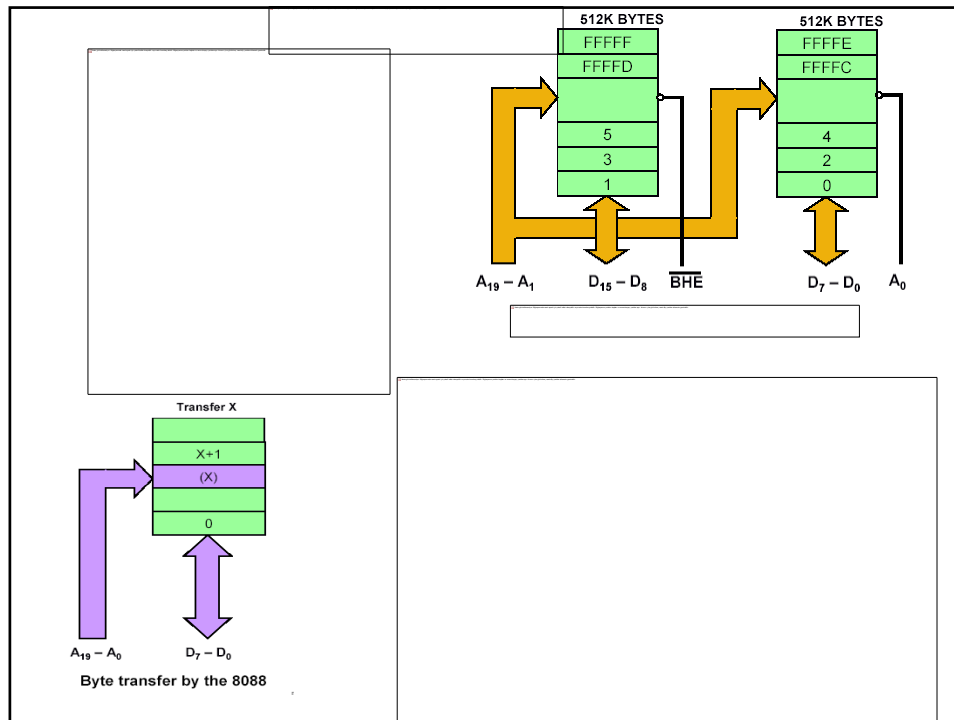
- First, the process of erasure of the entire contents takes less than a second, or one might say in a flash, hence its name: flash memory
- When flash memory's contents are erased, the entire device is erased.
- Even though flash memories are writeable, like EPROMs they find their widest use in microcomputer systems for storage of firmware

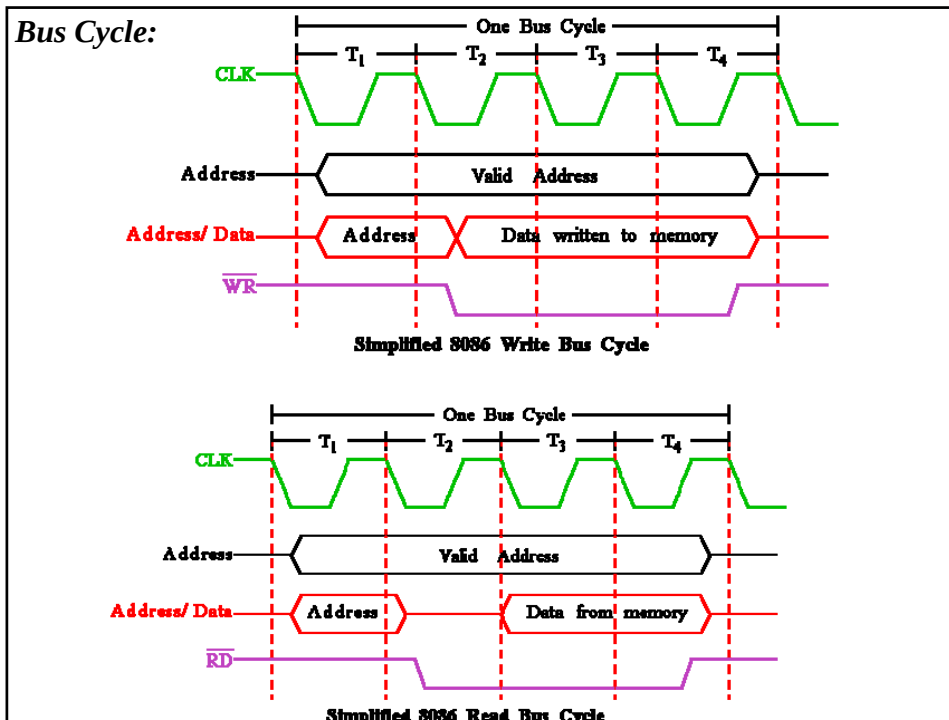
### ▸ RAM (Random Access Memory) infinite times

- RAM memory is called volatile memory since cutting off the power to the IC will mean the loss of data.
- Also referred to as R/W (Read And Write Memory)

Before a memory can be interfaced to the microprocessor, the pin connections on the memory must be understood so they can be properly connected to the microprocessor's address, data, and control bus signals. Recall from the last note that the address bus contains the memory address to select a location in the memory or I/O. It then sends the control signals to cause a read ( $\overline{RD}=0$ ) or a write ( $\overline{WR}=0$ ) and to select memory ( $\text{IO}/\overline{M}=0$ ) or I/O ( $\text{IO}/\overline{M}=1$ ). Finally data, from the data bus, are written to the memory or I/O or read from the memory or I/O. In other words, see chart below!

| <i>Operation</i> | $\overline{RD}$ | $\overline{WR}$ | $\text{IO}/\overline{M}$ |
|------------------|-----------------|-----------------|--------------------------|
| Memory Read      | 0               | 1               | 0                        |
| Memory Write     | 1               | 0               | 0                        |
| I/O Read         | 0               | 1               | 1                        |
| I/O Write        | 1               | 0               | 1                        |





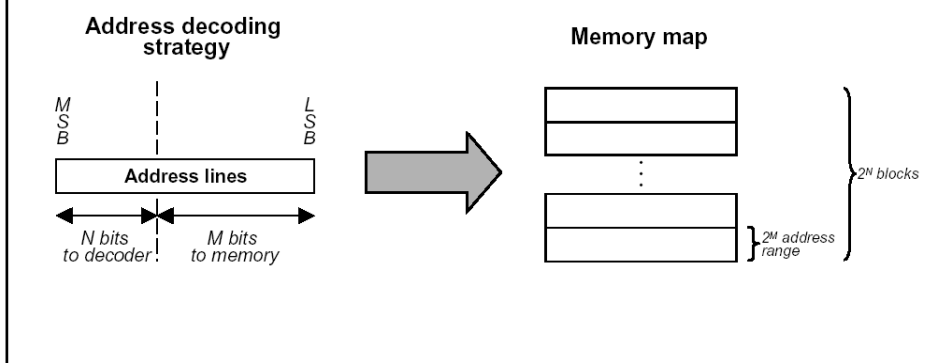
### Address decoding

**Address decoding** is the process of generating chip select ( $CS^*$ ) signals from the address bus for each device in the system. The address bus lines are split into two sections. The  $N$  most significant bits are used to generate the  $CS^*$  signals for the different devices.

The  $M$  least significant signals are passed to the devices as addresses to the different memory cells or internal registers.

### Memory Address Decoding

In order to splice a memory device into the address space of the processor, decoding is necessary.

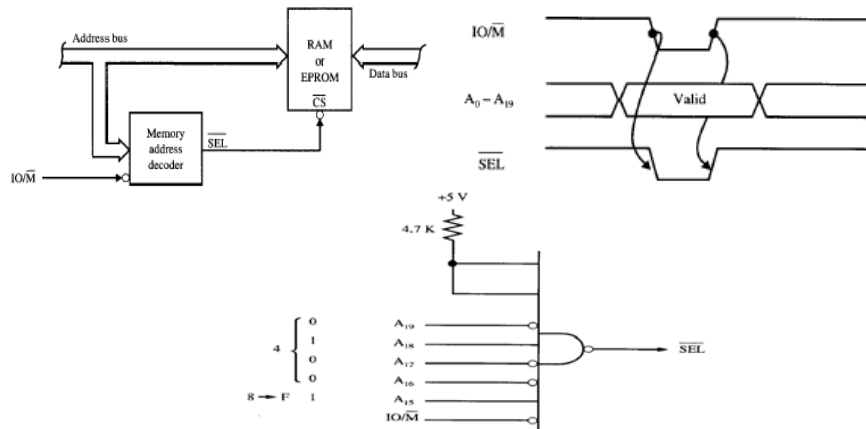


## Address decoding

CPU may interface with a number of memory ICs.

During a read/write operation, only the chip that stores the wanted data is enabled while the others are not.

**Memory address decoding** is to monitor the address bus and accordingly determine which of the memory chips is enabled.



## Address decoding: basic techniques

Each memory chip is responsible for a section of the memory space, which contains a number of locations.

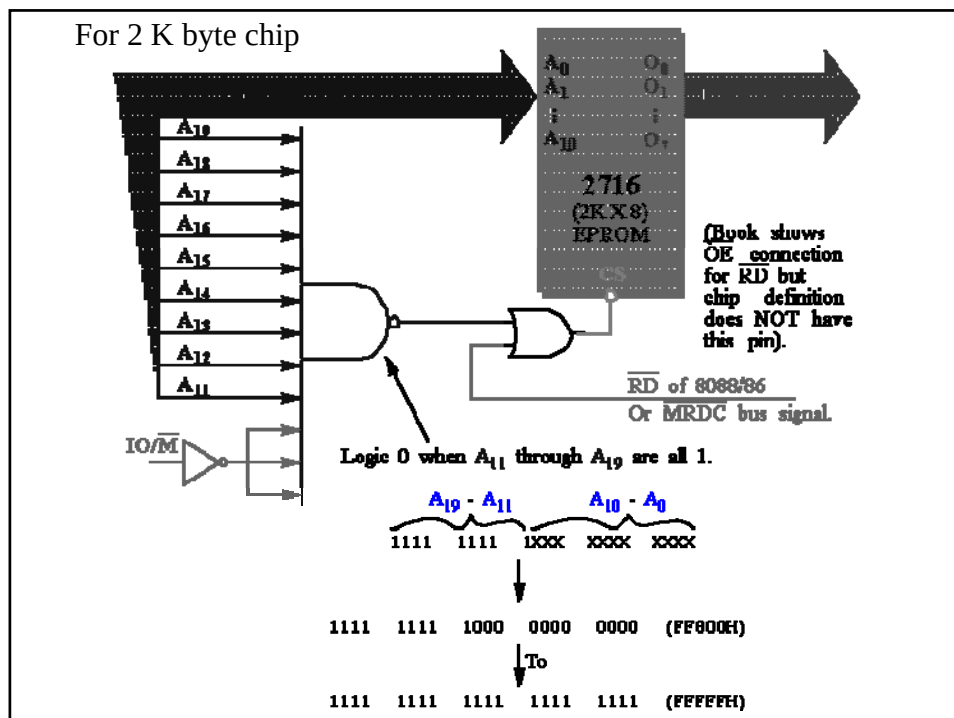
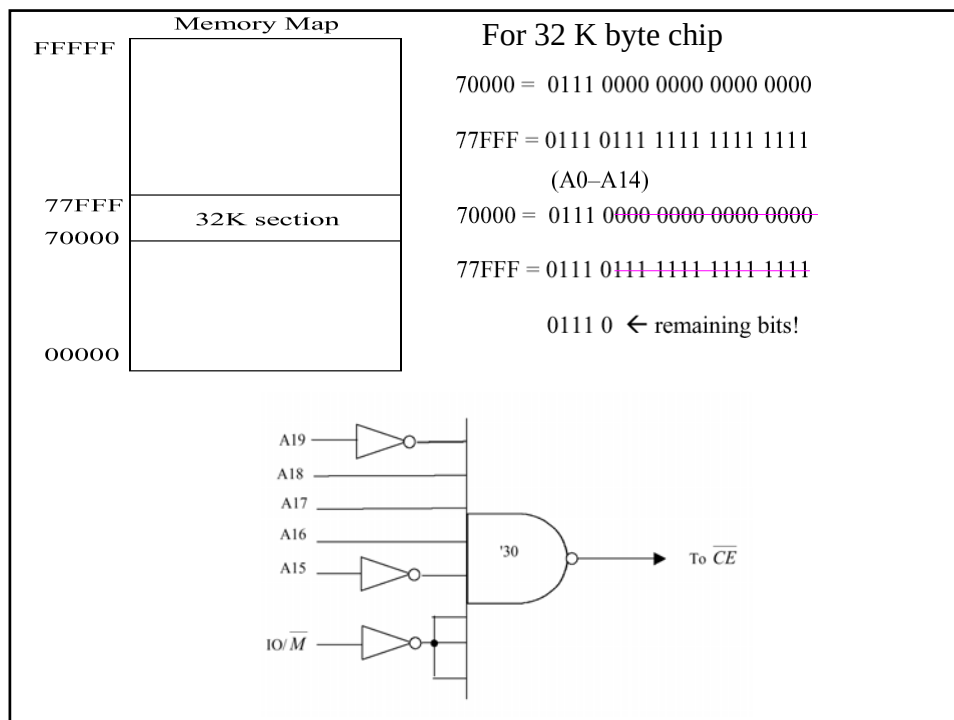
The higher bits of the address bus are used to select the chip while the lower bits identify the exact location in the chip.

For a 32 KB RAM device, 15 address lines are needed for accessing all of the 32 K locations in the chip.

In this case, A0 to A14 go directly into the RAM. A15 through A19 are used to determine where the 32 KB block is located in the entire 1 MB memory space.

If the RAM starts from address 48000H, the 20-bit address for any location in this chip must be

0100 1xxx xxxx xxxx xxxx



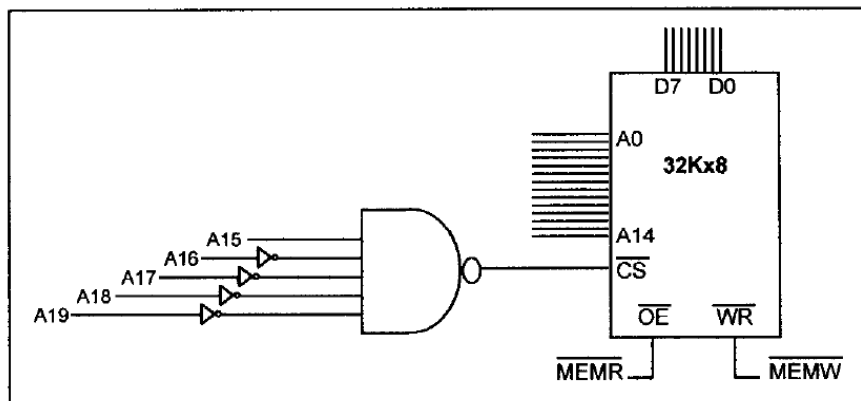
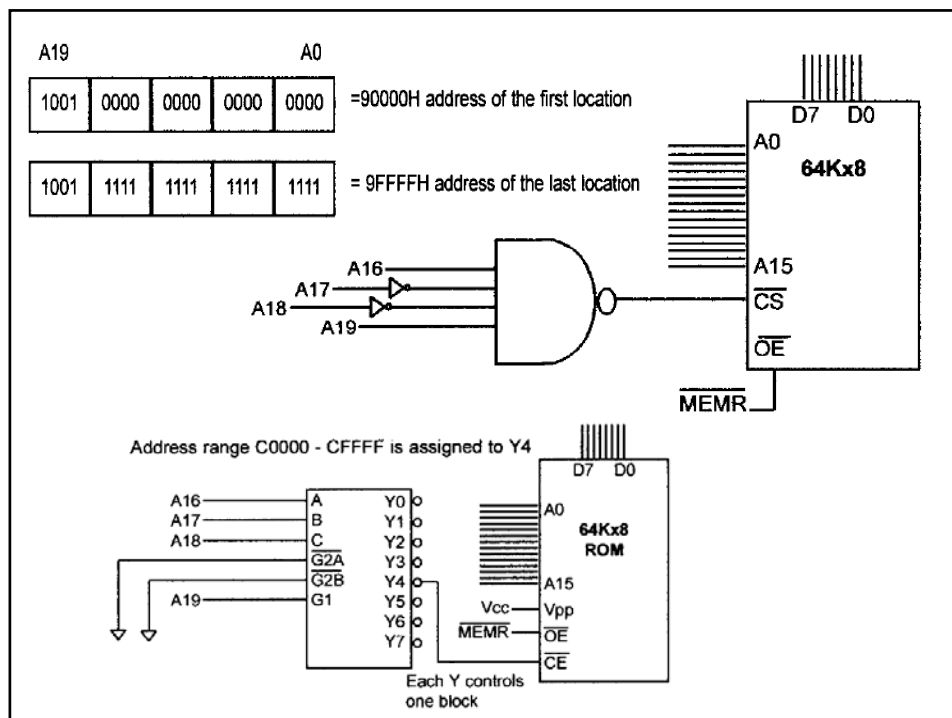
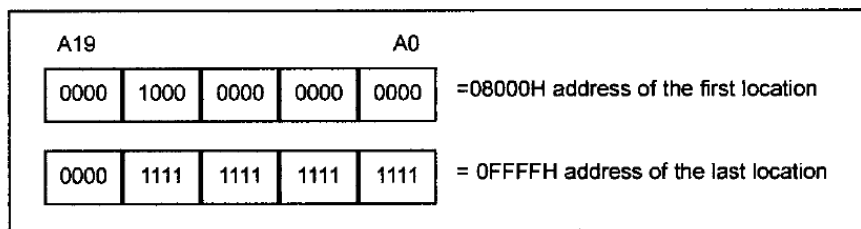
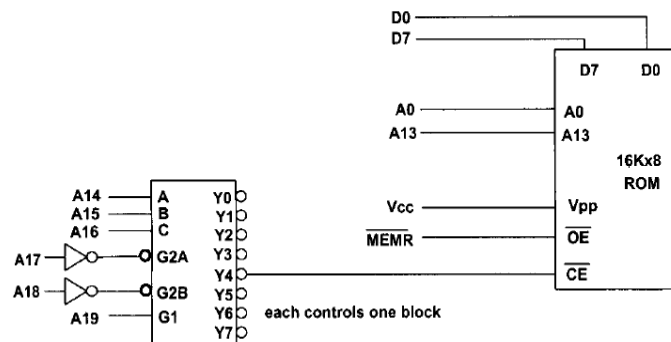


Figure 10-8. Using Simple Logic Gate as Decoder





## Address decoding using 74LS138



This decoder is functioning only when  $A_{17} = 1$ ,  $A_{18} = 1$  and  $A_{19} = 1$ .

That is, addresses being accessed are

111y yyxx xxxx xxxx xxxx

where the "yyy" are from  $A_{14} - A_{16}$ .  $A_0 - A_{13}$  are used to select the exact location within a memory chip.

In this example, Y4 is low when  $A_{14} = 0$ ,  $A_{15} = 0$  and  $A_{16} = 1$ . Thus the corresponding address range is  $F0000H - F3FFFH$ .

