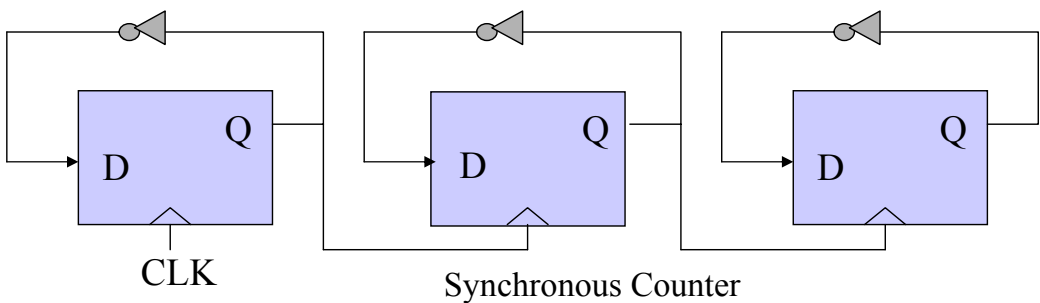
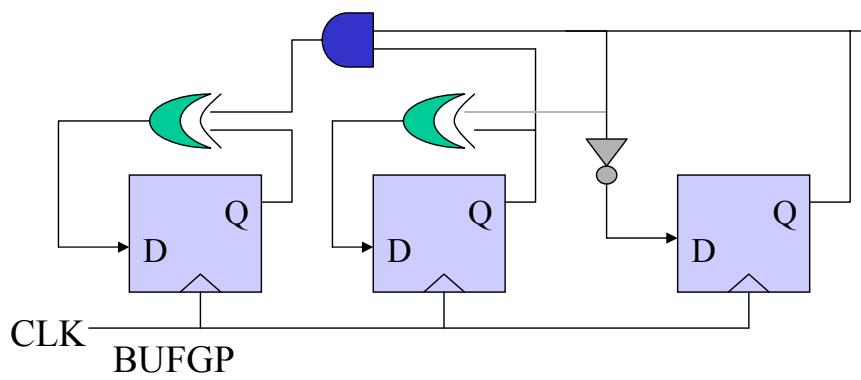


Counter and Timers: programmable Interval Timer 8253/54 Timer

Asynchronous Counter



Synchronous Counter



Creating time delays in 8088/8086 based system for a delay loop

```
MOV CX,N
```

Again: LOOP again

Every loop takes total of 17 clock pulse to be executed so the time delay is $N \times 17$ example : system frequency is 4.7 MHz ($t = 210$ ns). For 100ms delay its needed $N = 28000$

another way for delay generation is using of external hardware timers

Programmable Interval Timer - 8254

The 8254 programmable interval timer consists of three independent 16-bit programmable counters (**timers**).

Each counter is capable in of counting in binary or BCD with a maximum frequency of 10MHz.

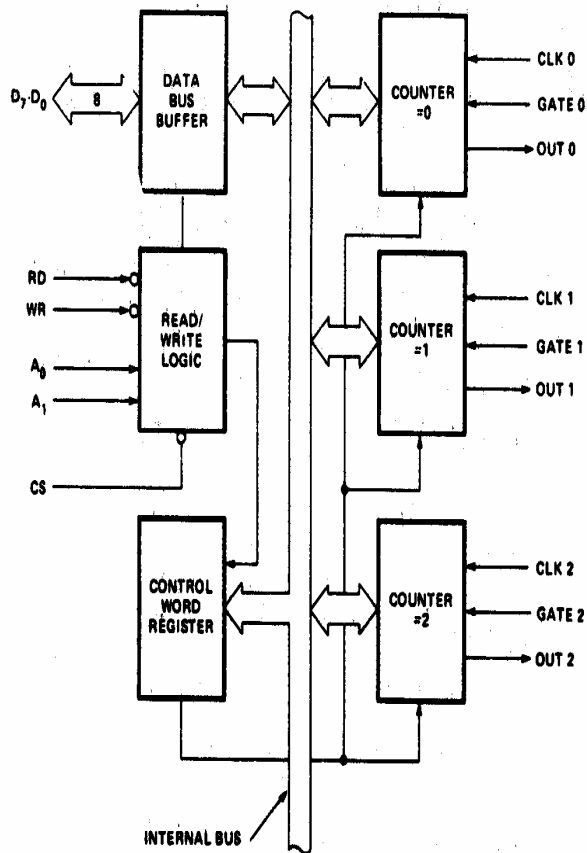
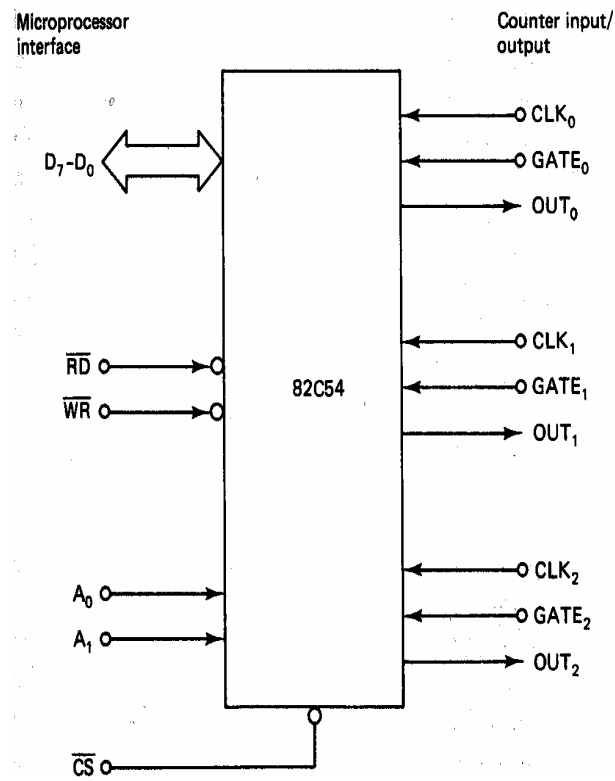
Used for controlling real-time events such as real-time clock, events counter and motor speed and direction control.

Usually decoded at port address 40H-43H and has following functions:

- Generate a basic timer interrupt that occurs at approximately 18.2Hz.
- Cause the DRAM memory system to be refreshed
- Providing a timing source to the internal speaker and other devices.

Programmable Timer

Internal architecure of the 82C54



CLK

CLK is the input clock frequency, which can range between 0 and 2 MHz for the 8253. for input frequencies higher than 2 MHz, the 8254 must be used; the 8254 can go as high as 8 MHz, and the 8254-2 can go as high as 10 MHz.

OUT

Although the input frequency is a square wave of 33% duty cycle, the shape of the output frequency coming from the OUT pin after being divided can be programmed. Among the options are square-wave, one-shot, and other square-shape waves of various duty cycles but no sine-wave or saw-tooth shapes.

GATE

This pin is use to enable or disable the counter. Putting HIGH (5 V) on GATE enables the counter, whereas LOW (0 V) disables it in some modes a 0-to-1 pulse must be applied to GATE to enable the counter.

D0 – D7

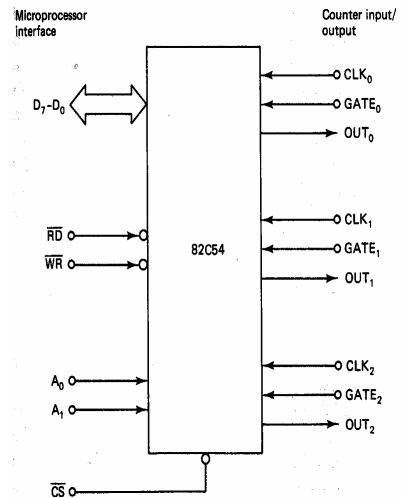
The D0 –D7 data bus of the 8253/54 is a bidirectional bus connected to D0 –D7 of the system data bus. The data bus allows the CPU to access various registers inside the 8253/54 for both read and write operations. RD and WR (both active low) are connected to IOR and LOW control of the system bus.

Pin Description of 8253/54

A0, A1, and $\overline{\text{CS}}$

- Inside the 8253/54 timer, there are 3 counters.
- Each timer works independently and programmed separately.
- Each counter is assigned an individual port address.
- The control register common to all 3 counters and has its own port.

CS	A1	A0	Port
0	0	0	Counter 0
0	0	1	Counter 1
0	1	0	Counter 2
0	1	1	Control register
1	x	x	8253/54 is not selected



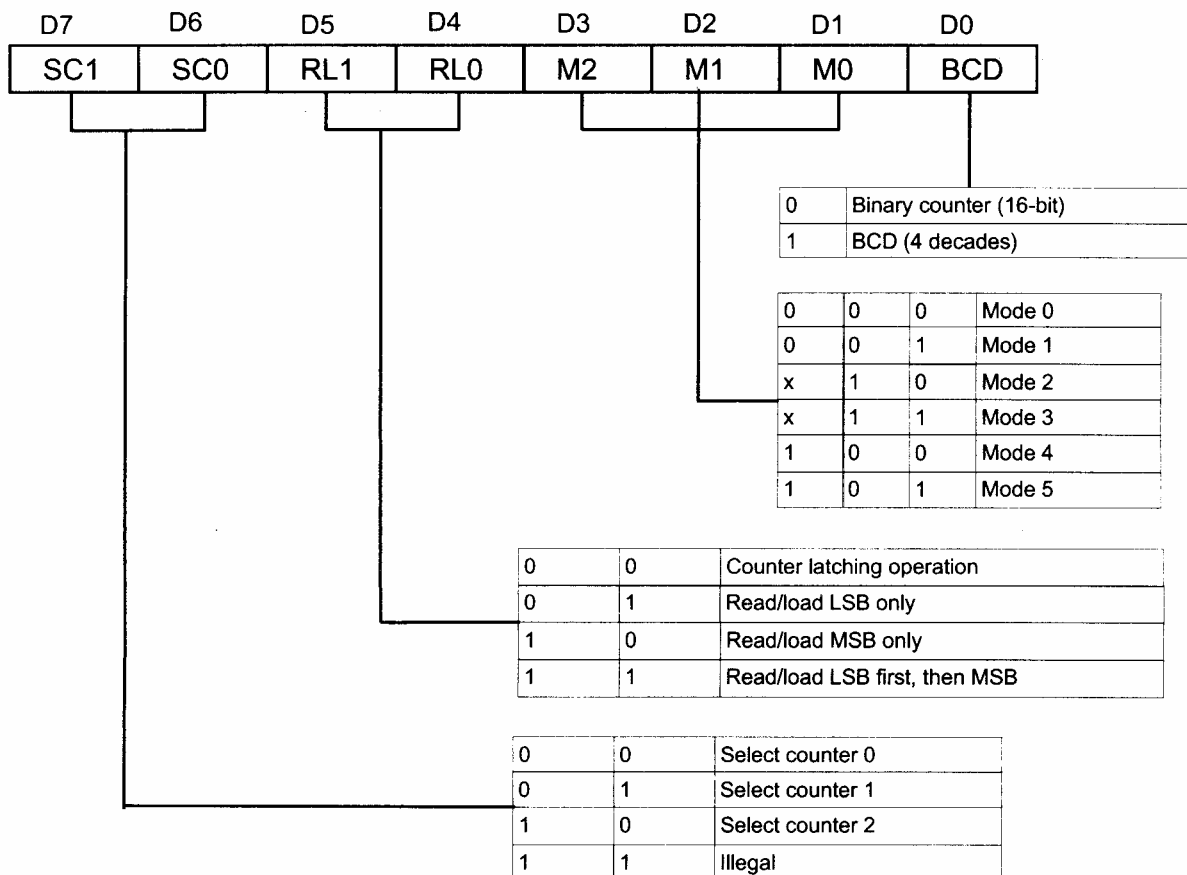


Figure 5-2. 8253/54 Control Word Format

Example 5-1

Pin $\overline{CS}$ of a given 8253/54 is activated by binary address A7 - A2 = 100101.

(a) Find the port addresses assigned to this 8253/54.

(b) Find the configuration for this 8253/54 if the control register is programmed as follows.

```
MOV  AL,00110110
OUT  97H,AL
```

Solution:

(a) From Table 5-1, we have the following:

<u>CS</u>	<u>A1A0</u>	<u>Port</u>	<u>Port address (hex)</u>
1001 01	00	Counter 0	94
1001 01	01	Counter 1	95
1001 01	10	Counter 2	96
1001 01	11	Control register	97

(b) Breaking down the control word 00110110 and comparing it with Table 5-1 indicates counter 0 since the SC bits are 00. The RL bits of 11 indicates that the low-byte read/write is followed by the high byte. The mode selection is mode 3 (square wave), and finally binary counting is selected since the D0 bit is 0.

Control word format

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
SC ₁	SC ₀	RW/W ₁	RW/W ₀	M ₂	M ₁	M ₀	BCD

Definition of control

SC-select counter:

SC ₁	SC ₀	
0	0	Select counter 0
0	1	Select counter 1
1	0	Select counter 2
1	1	Read back command

RW-read/write:

RW/W ₁	RW/W ₀	
0	0	Counter latch command
1	0	Read/write most significant byte only
0	1	Read/write least significant byte only
1	1	Read/write least significant byte first, then most significant byte

M-mode:

M ₂	M ₁	M ₀	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD:

0	Binary counter 16-bits
1	Binary coded decimal (BCD) counter (4 decades)

Control word format of the 82C54

Operation Modes (Six operation modes)

Mode 0 Interrupt on terminal count

Mode 1 Programmable one-shot

Mode 2 Rate Generator

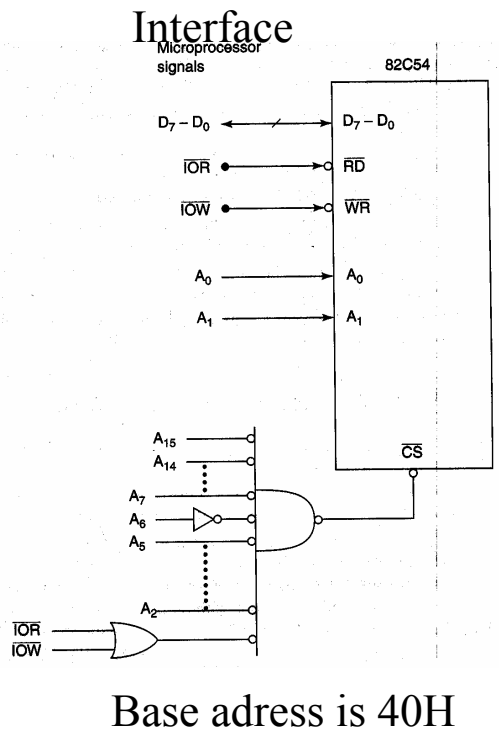
Mode 3 Square wave rate generator

Mode 4 Software triggered strobe

Mode 5 Hardware trigger strobe

Accessing the register of the 82C54

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (3-State)
1	X	X	X	X	No-Operation (3-State)
0	1	1	X	X	No-Operation (3-State)



Example: Bsed on last figure load : counter0=1234H, Binary counter in mode 0 Counter1 =0100h, BCD counter in mode 2 counter 2=1FFFh Binary counter in mode3	MOV	AL, 30H ; set up counter 0
	OUT	43H, AL
	MOV	AL, 55H ; set up counter 1
	OUT	43H, AL
	MOV	AL, B8H; set up counter 2
	OUT	43H, AL
	MOV	AL,34H; load counter 0 with 1234H
	OUT	40H, AL
	MOV	AL,12H
	OUT	40H, AL
	MOV	AL,00H; load counter 1 with 100H
	OUT	41H, AL
	MOV	AL,01H
	OUT	41H, AL
	MOV	AL,FFH; load counter 2 with 1FFFH
	OUT	42H, AL
	MOV	AL,1FH
	OUT	42H, AL

Content of each register could be read at any time.

Methods of reading the state of a counter while counting :

1-Employ a read from the input port associated with the counter.

The counter must be temporarily paused.

2-Using the 8254's counter latch command. This command is selected by clearing bits 5 and 4 in the control word for a particular counter. This causes the 8254 to transfer a copy of the selected count register into an output latch

3-The third technique uses a read-back command to read the state of 3counter with a single command. The read-back command is issued by setting bits 7 and 6 .

Example: Write an instruction sequence to read the contebt of counter 2. The content is to be loaded into the AX register. The base adress of timer is 40H . (latch command)

Mov AL, 1000xxxxB

OUT 43 H, AL

IN AL, 42H

MOV BL,AL; READ THE LOW BYTE

IN AL,42H, READ THE HIGH BYTE

MOV AH,AL

MOV AL,BL, AX =COUNTER2 VALUE

Mode 0: interrupt on terminal count

The output in this mode is initially low, and will remain low for the duration of the count if $GATR = 1$. The width of the low output is as follows.

Width of low pulse = $N \times T$

Where N is the clock count loaded into counter, and T is the clock period of the CLK input. When the terminal count is reached, the output will go high and remain high until a new control word or new count number is loaded.

Mode 1: programmable one-shot

This mode is also called **hardware triggerable one-shot**. The triggering must be done through the GATE input by sending a 0-to-1 pulse to it. In 8253/54 modes that are programmable (triggerable) such as mode 1, the following two steps must be performed for the counter to work.

1. Load the count register.
2. A 0-to-1 pulse must be sent to the GATE input to trigger the counter.

Mode 2: rate generator

Mode 2 is also called **divide-by-N counter**. In this mode, if $GATE = 1$, OUT will be high for the $N \times T$ clock period, goes low only for one clock pulse, then the count is reloaded automatically, and the process continues indefinitely. This mode in effect produces a divide-by-N counter. In this mode, the period of OUT is equal to $(N + 1) \times T$ where for $N \times T$, OUT is high and 1 clock pulse, OUT is low.

Mode 3: square wave rate generator

In this mode if $GATE = 1$, OUT is a square wave the high pulse is equal to the low pulse if N is an even number. In that case, the high part and low part of the pulse have the same duration and are equal to $(N/2) \times T$ where N is the clock count and T is the CLK period. In this mode, the count is reloaded automatically when the terminal count is reached, thereby producing a continuous square wave with frequency of $1/N$ of the CLK frequency. Mode 3 is similar to mode 2, except that OUT in mode 3 is a square wave of 50% duty cycle. If an odd number is loaded into counter, the time for high position is $(N+1)/2$ and the time for low position is $(N-1)/2$

Mode 4: software triggered strobe

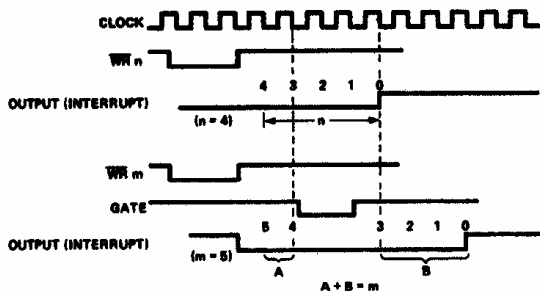
In this mode if $GATE = 1$, the output will go high upon loading the count. It will stay high for the duration of $N \times T$, where N is the count and T is the clock period. After the count reaches zero (terminal count), it becomes low for one clock pulse, then goes high again and stays high until a new command word or new count is loaded. To repeat the strobe, the count must be reloaded again. In other words, this mode does not automatically reload the count upon reaching the terminal count.

Mode 4 is similar to mode 2, except the counter is not reloaded automatically. In this mode, if the GATE input becomes low, the count will stop and the output will be high. The count resumes only when the gate becomes high again.

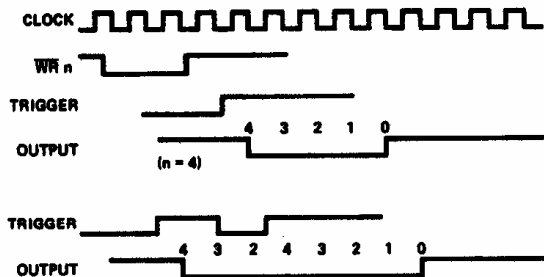
Mode 5: hardware triggered storbe

This mode is similar to mode 4 except the triggering must be done with the GATE input. In this mode, the count begins only when a 0-to-1 pulse is sent to the GATE input. This is unlike mode 4 where the counter started upon loading the count, as $GATE = 1$.

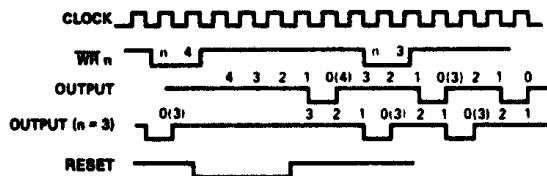
MODE 0: INTERRUPT ON TERMINAL COUNT



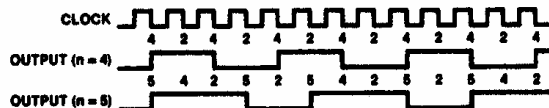
MODE 1: PROGRAMMABLE ONE-SHOT



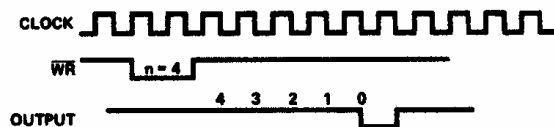
MODE 2: RATE GENERATOR



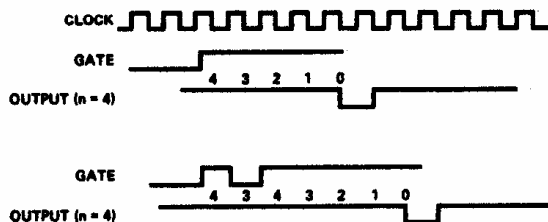
MODE 3: SQUARE WAVE GENERATOR



MODE 4: SOFTWARE TRIGGERED STROBE



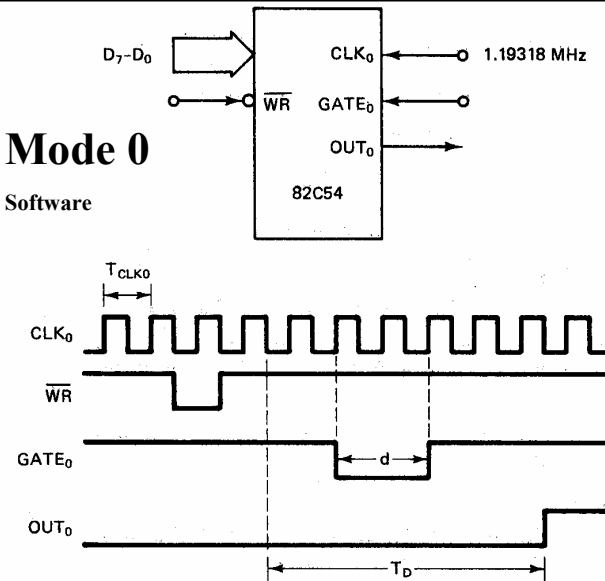
MODE 5: HARDWARE TRIGGERED STROBE



Operating modes of 82C54

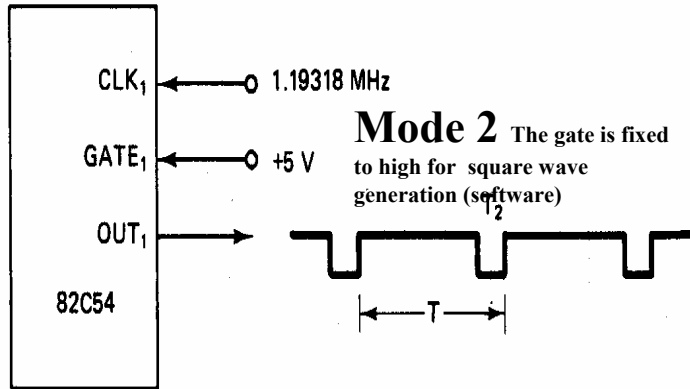
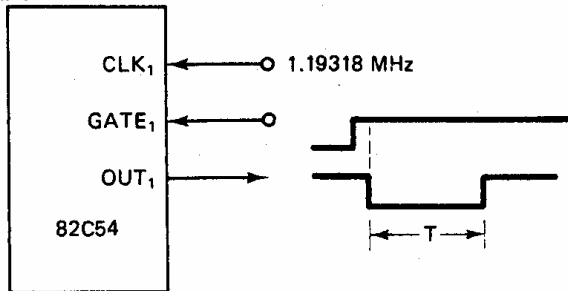
Mode 0

Software

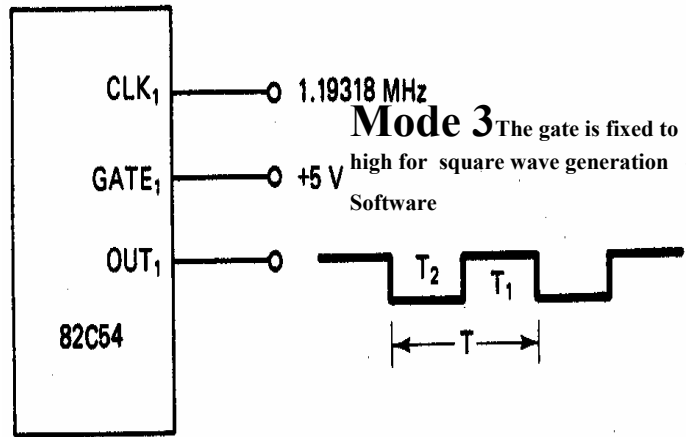


Mode 1

Hardware

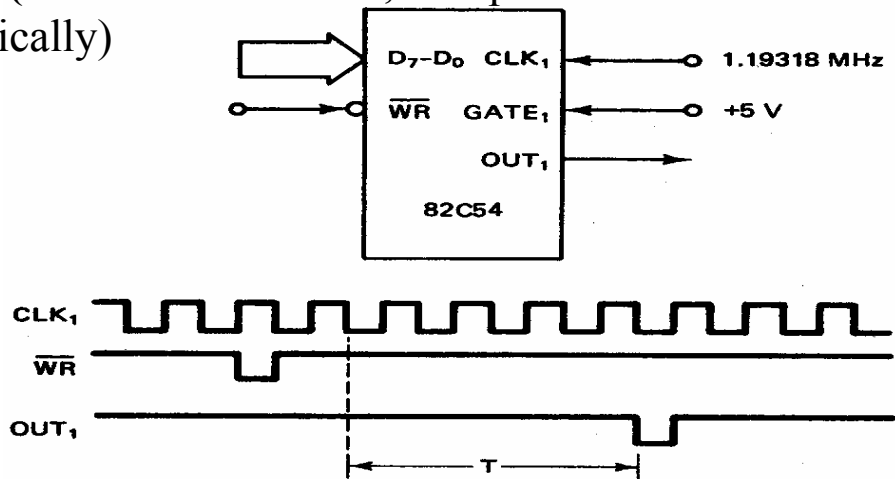


Mode 2 The gate is fixed to high for square wave generation (software)

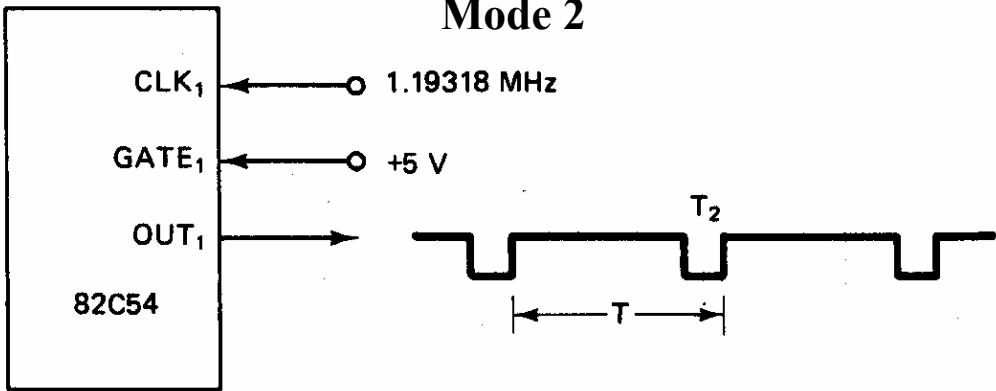


Mode 3 The gate is fixed to high for square wave generation (software)

Mode 4 (is similar to mode 2, except the counter is not reloaded automatically)



Mode 2



Example 5-2

Address of Counter0=94H, Counter 1 =95H, Counter2=96H, Control register=97H

- (a) counter 0 for binary count of mode 3 (square wave) to divide CLK0 by number 4282 (BCD)
- (b) counter 2 for binary count of mode 3 (square wave) to divide CLK2 by number C26A hex
- (c) Find the frequency of OUT0 and OUT2 in (a) and (b) if CLK0 =1.2 MHz, CLK2 = 1.8 MHz.

Solution:

- (a) To program counter 0 for mode 3, we have 00110111 for the control word. Therefore,

```
MOV  AL,37H      ;counter 0, mode 3, BCD
OUT  97H,AL      ;send it to control register
MOV  AX,4282H    ;load the divisor (BCD needs H for hex)
OUT  94H,AL      ;send the low byte
MOV  AL,AH       ;to counter 0
OUT  94H,AL      ;and then the high byte to counter 0
```

- (b) By the same token:

```
MOV  AL,B6H      ;counter2, mode 3, binary(hex)
OUT  97H,AL      ;send it to control register
MOV  AX,C26AH    ;load the divisor
OUT  96H,AL      ;send the low byte
MOV  AL,AH       ;to count 2
OUT  96H,AL      ;send the high byte to counter 2
```

- (c) The output frequency for OUT0 is 1.2MHz divided by 4282, which is 280 Hz. Notice that the program in part (a) used instruction "MOV AX,4282H" since BCD and hex numbers are represented in the same way, up to 9999. For OUT2, CLK2 of 1.8 MHz is divided by 49770 since C26AH = 49770 in decimal. Therefore, OUT2 frequency is a square wave of 36 Hz.

Example 5-3

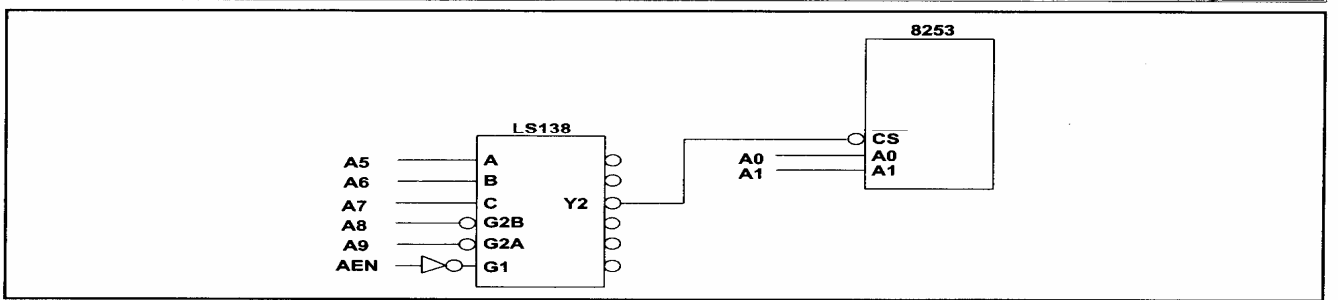
Using the port addresses in Example 5-1, show the programming of counter 1 to divide CLK1 by 10,000, producing the mode 3 square wave. Use the BCD option in the control byte.

Solution: Address of Counter0=94H, Counter 1 =95H, Counter2=96H, Control register=97H

MOV	AL,77H	;counter1, mode 3, BCD
OUT	97H,AL	;send it to control register
SUB	AL,AL	;AL =0 load the divisor for 10,000
OUT	95H,AL	;send the low byte
OUT	95H,AL	;and then the high byte to counter 1

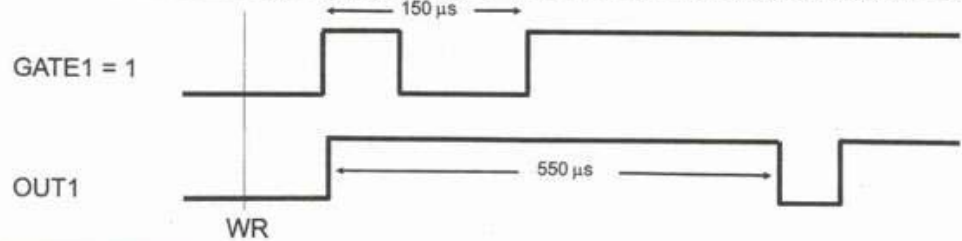
8253/54 Timer Connections and Programming (address decoding)

Binary Address										Hex Address	Function	
AEN	A9	A8	A7	A6	A5	A4	A3	A2	A1			A0
1	0	0	0	1	0	x	x	x	0	0	40	Counter 0
1	0	0	0	1	0	x	x	x	0	1	41	Counter 1
1	0	0	0	1	0	x	x	x	1	0	42	Counter 2
1	0	0	0	1	0	x	x	x	1	1	43	Control register



In Example 13-13, assume that GATE1 is retriggered after 150 pulses. Show the output for OUT1.

Solution:
If GATE1 is retriggered after 150 clock pulses into the countdown, COUNT1 is reloaded with N = 400 and the counts begins again, making the OUT1 pulse duration 550 μ s, as shown next.

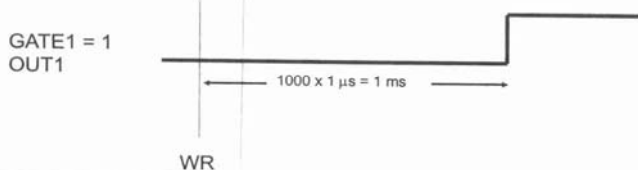


Example 13-7

Assume that $GATE1 = 1$ and $CLK1 = 1 \text{ MHz}$, and the clock count $N = 1000$. Show the output of $OUT1$ if it is programmed in mode 0.

Solution:

The clock period of $CLK1$ is $1 \mu\text{s}$; therefore, $OUT1$ is low for $1000 \times 1 \mu\text{s} = 1 \text{ ms}$, before it goes high, as shown in the following diagram.



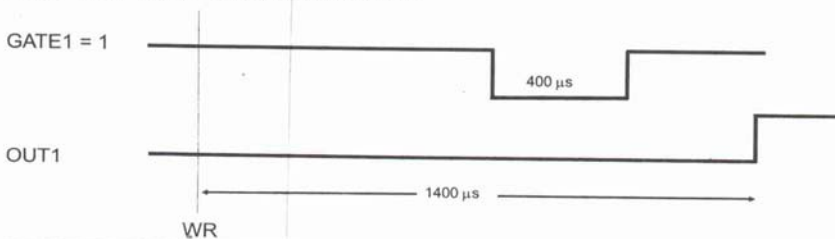
In this mode, if the $GATE$ input becomes low at the middle of the count, the count will stop and the output will be low. The count resumes when the gate becomes high again. This in effect adds to the total time the output is low. The amount added is the time that the $GATE$ input was kept low.

Example 13-8

In Example 13-7, assume that $GATE1$ becomes zero for $400 \mu\text{s}$. What is the width of the low pulse for $OUT1$?

Solution:

It is $1000 \mu\text{s} + 400 \mu\text{s} = 1400 \mu\text{s}$, as shown next.



Mode 1: programmable one-shot

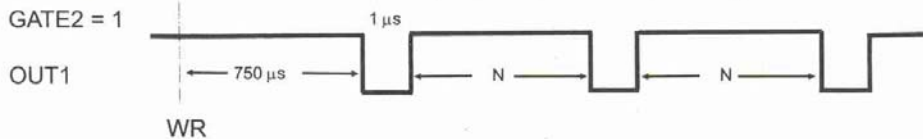
Mode 2

Example 13-10

If CLK2 = 1 MHz, GATE2 = 1, and N = 750, show OUT2 if COUNT2 is programmed for mode 2.

Solution:

Notice that the count is reloaded automatically and the counter continues to produce OUT2.



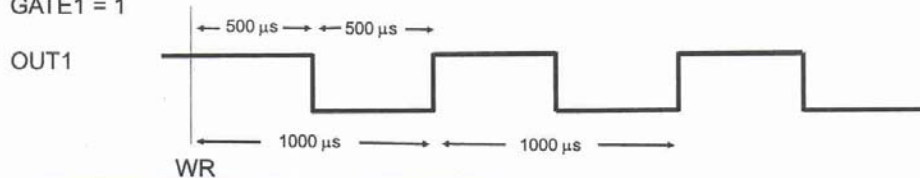
Mode 3

If CLK2 = 1 MHz, GATE1 = 1, N = 1000, show OUT1 if COUNT1 is programmed for mode 3.

Solution:

Since the clock period is 1 μ s, OUT1 is high for 500 μ s and low for 500 μ s, producing the square wave of 1 ms period continuously, as shown next.

GATE1 = 1



count will resume only after GATE = 1. See Example 13-11.

Example 13-12

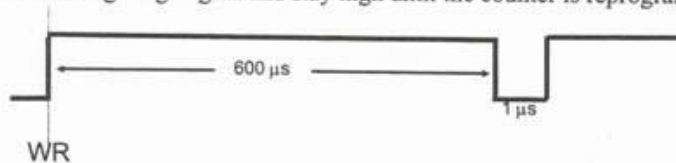
If $\text{CLK0} = 1 \text{ MHz}$, $\text{GATE0} = 1$, and $N = 600$, show the shape of OUT0 where counter 0 is programmed for mode 4.

Solution:

Mode 4

Since the CLK0 period is $1 \mu\text{s}$, after the count is loaded OUT0 will be high for $600 \mu\text{s}$ and will go low for $1 \mu\text{s}$. Then it will go high again and stay high until the counter is reprogrammed, as shown below.

$\text{GATE0} = 1$
 OUT0

**Example 13-13**

If $\text{CLK1} = 1 \text{ MHz}$, and $N = 400$, show the output for OUT1 if it is programmed for mode 5.

Solution:

Mode 5

Notice that the count starts only when the 0-to-1 pulse is applied to GATE1 .

$\text{GATE1} = 1$

OUT1

